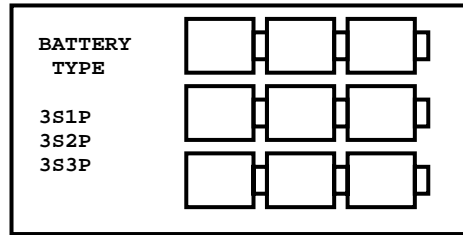


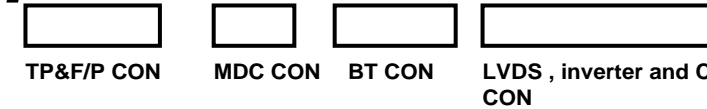
sualaptop365.edu.vn

<Variant Name>			
		Title : PAGE REF.	
ASUSTek COMPUTER INC		Engineer: <i>Kent Qi</i>	
Size Custom	Project Name F6Ve		Rev 1.0
Date: Friday, September 26, 2008		Sheet 1 of 64	

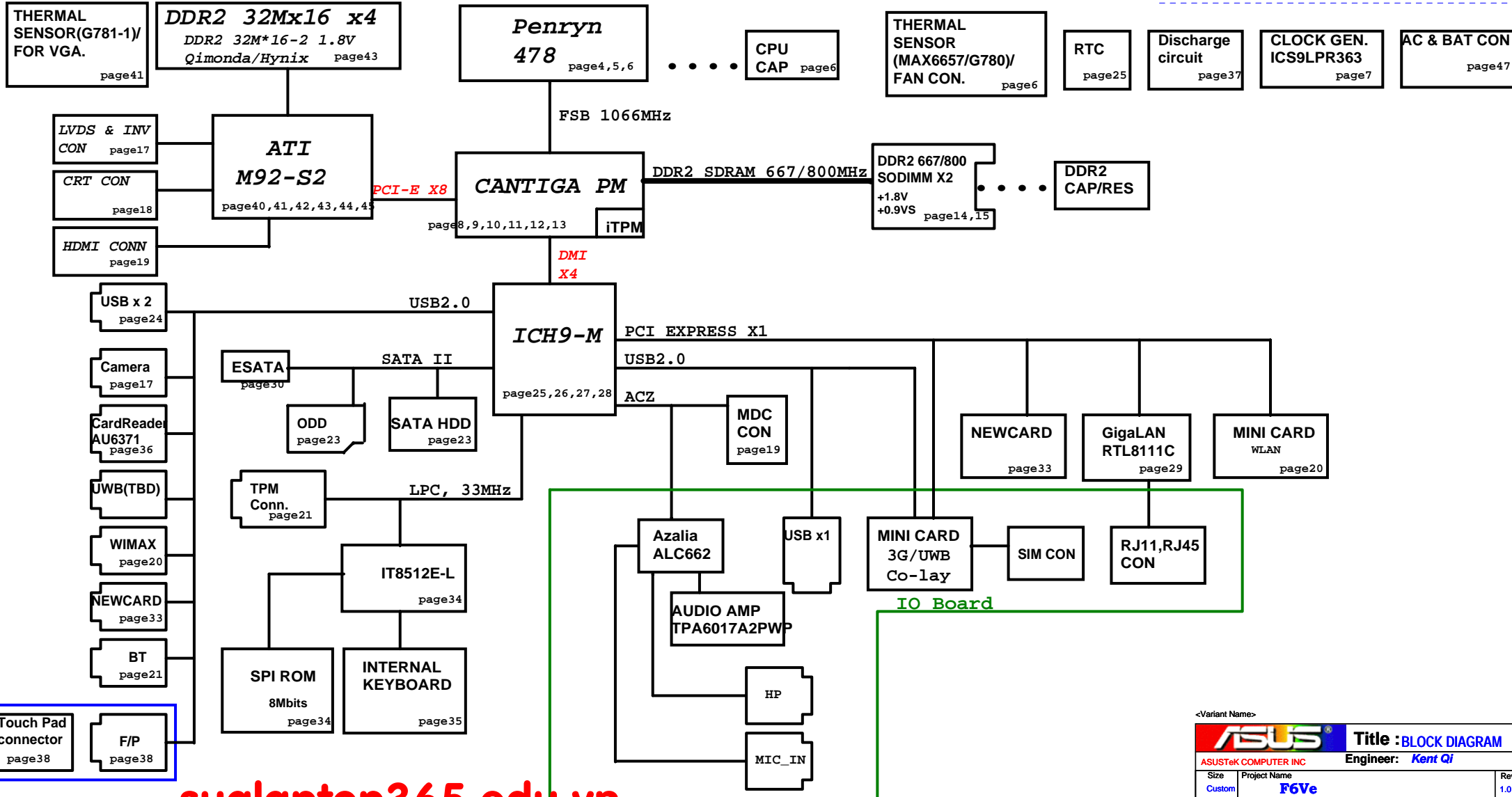
F6Ve BLOCK DIAGRAM



Internal IO CON with Cable for MB



Internal IO CON with Cable for IO Board



<Variant Name>

EC IT8512

EC GPIO	Use As	Signal Name	Power
GP0	GPO	PWR_LED#	
GP1	GPO	CHG_LED#	
GP2	GPO	BATSEL_3S#	
GP3	-	-	
GP4	GPO	LCD_BL_PWM	
GP5	GPO	FAN0_PWM	
GP6	-	-	
GP7	-	-	
GP8	GPO	CHG_EN#	
GP9	GPO	PRECHG	
GP10	-	-	
GP11	ALT	SMB0_CLK _{Battery}	
GP12	ALT	SMB0_DAT	
GP13	OD	A20GATE	
GP14	OD	RCIN#	
GP15	GPO	PM_RSMRST#	
GP16	-	-	
GP17	ALT	SMB1_CLK _{ThermalSensor}	
GP18	ALT	SMB1_DAT	
GP19	GPO	PM_PWRBTN#	
GP20	GPI	AC_IN_OC#	
GP21	GPO	OP_SD#	
GP22	GPI	BAT1_IN_OC#	
GP23	GPI	RFON_SW#	
GP24	GPI	PWRLIMIT#	
GP25	GPI	PM_SUSC#	
GP26	ALT	BUF_FLT_RST#	
GP27	OD	EXT_SCI#	
GP28	OD	EXT_SMI#	
GP29	GPO	LCD_BACKOFF#	
GP30	GPI	FAN0_TACH	
GP31	GPO	SD_CD#_EC	
GP32	GPO	VSUS_ON	
GP33	GPO	SUSC_EC#	
GP34	GPO	SUSB_EC#	
GP35	GPO	CPU_VRON	
GP36	GPI	PWR_SW#	
GP37	-	-	
GP38	GPI	LID_SW#	
GP39	-	-	
GP40	-	-	
GP41	-	-	
GP42	GPI	MARATHON#	
GP43	-	-	
GP44	ALT	TP_CLK	
GP45	ALT	TP_DAT	
GP46	GPO	THRO_CPU	
GP47	-	-	
GP48	GPO	PM_THERM#_EC	
GP49	GPI	PM_SUSB#	
GP50	-	-	
GP51	-	-	
GP52	-	-	

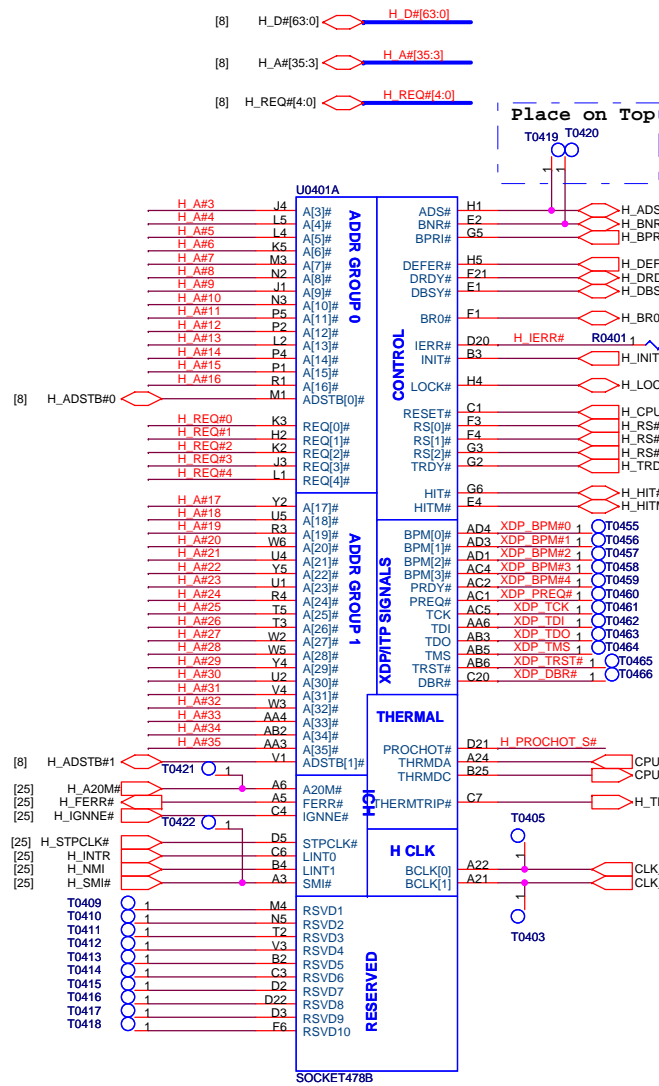
EC GPIO	Use As	Signal Name	Power
-	-	-	-
GP6	-	-	-
-	-	-	-
GP0	OD	PM_CLKRUN#	-
GP1	GPO	3G_ON#	-
GP2	-	-	-
GP3	GPO	BAT_LEARN	-
GP4	-	-	-
GP5	-	-	-
GP6	GPO/OD	CAP_LED#	-
-	-	-	-
GP10	GPI	VGA_ALERT#	-
GP11	GPI	SUS_PWRGD	-
GP12	GPI	ALL_SYSTEM_PWRGD	-
GP13	GPI	VRM_PWRGD	-
GP14	GPI	PWR_MON	-
GP15	-	-	-
GP16	GPI	KB_ID0(NC)	-
GP17	GPI	KB_ID1(NC)	-
GP0	GPO	EC_CLK_EN	-
GP1	GPO	PM_PWROK	-
GP2	GPI	-	-
GP3	GPO	BATSEL_2P#	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
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GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
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GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
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GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
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GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-
GP2	-	-	-
GP3	-	-	-
GP4	-	-	-
GP5	-	-	-
GP0	-	-	-
GP1	-	-	-

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1100001x (A2)
Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	UWB(TBD)
PCIE 6	LAN

SATA 0	SATA HDD
SATA1	SATA ODD
SATA4	
SATA5	ESATA

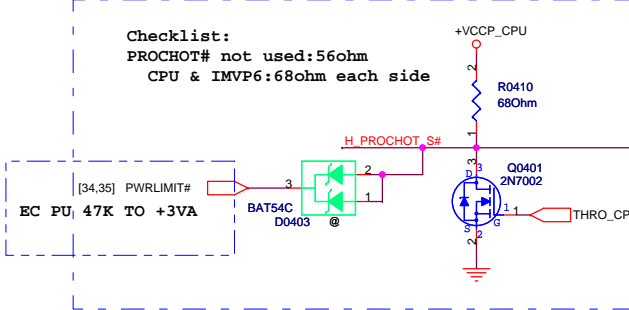
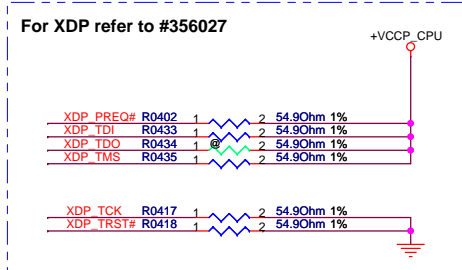
USB 0	USB Conn
USB 1	
USB 2	USB Conn
USB 3	USB Conn
USB 4	CMOS Camera
USB 5	CardReader
USB 6	UWB(TBD)
USB 7	WiMax
USB 8	NewCard
USB 9	3G Card
USB 10	Bluetooth
USB 11	FINGER PRINT



Zo=55 Ohm, 0.5" max
for GTL_REF

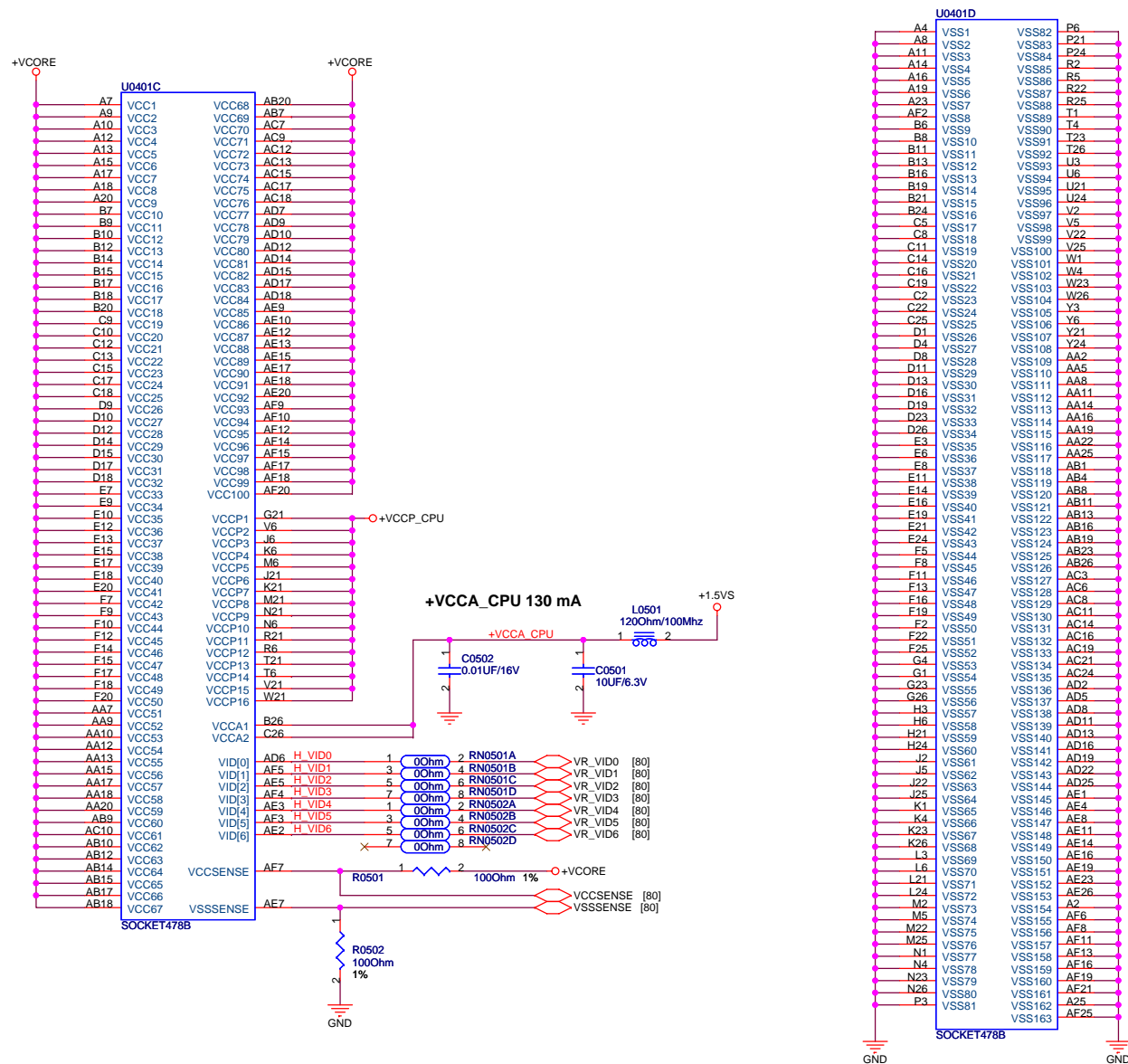
C0466
TEST4:CRB 0.1u Reserved
DG & Checklist:NC

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

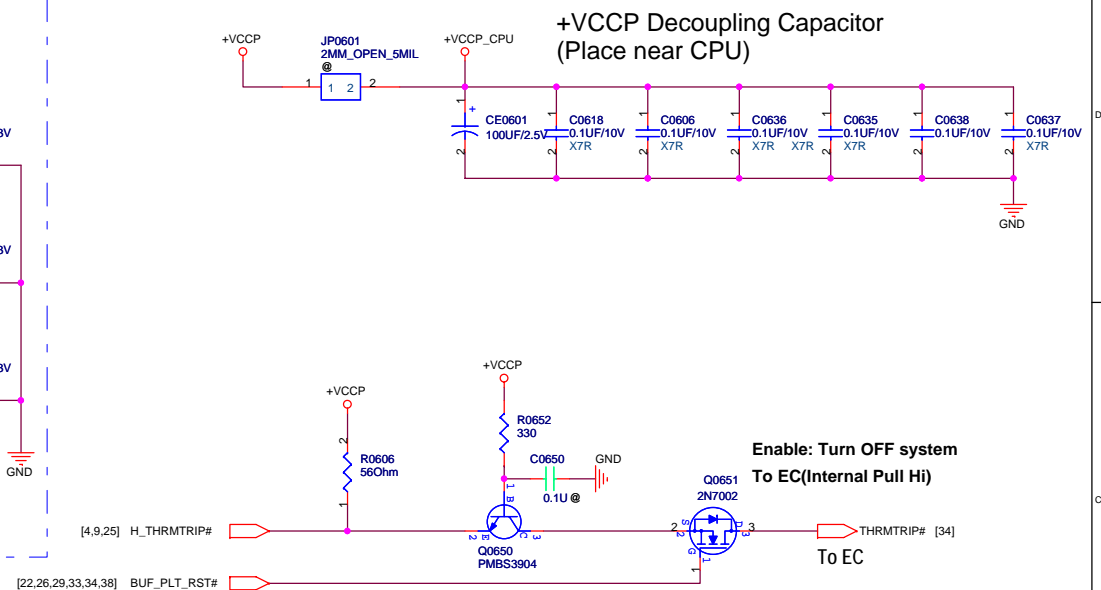
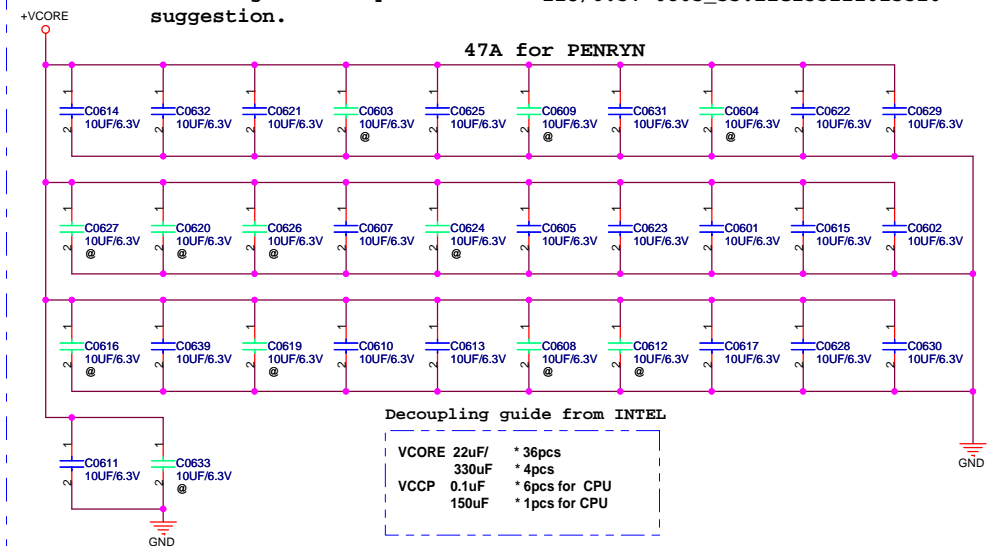


Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: ZO=55 Ohm, trace length < 0.5"

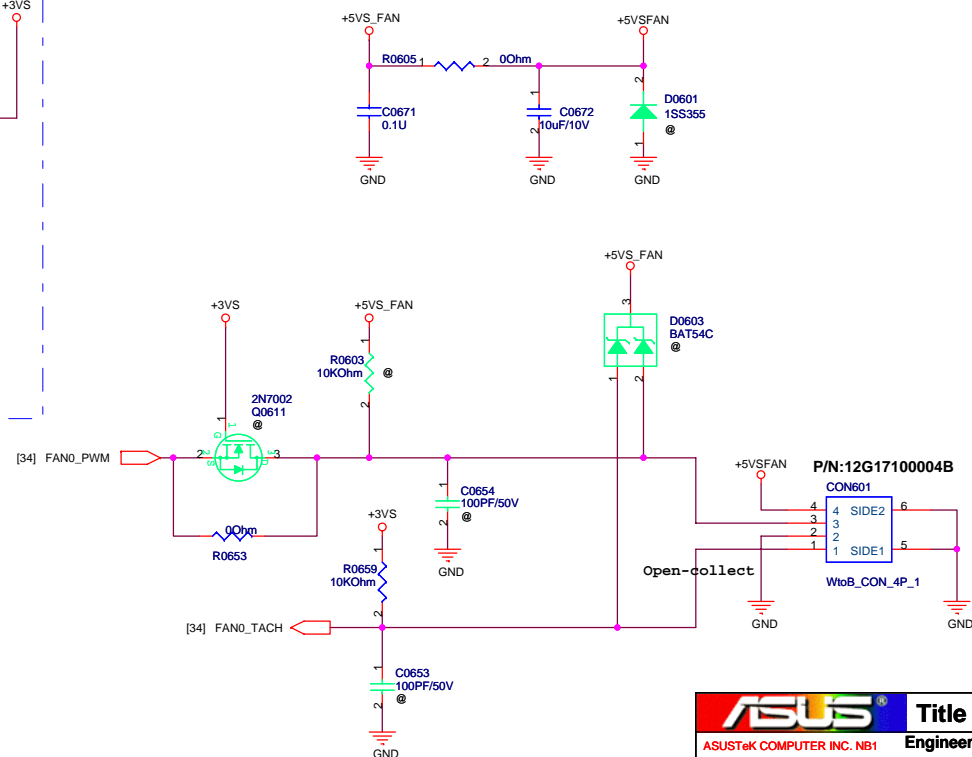
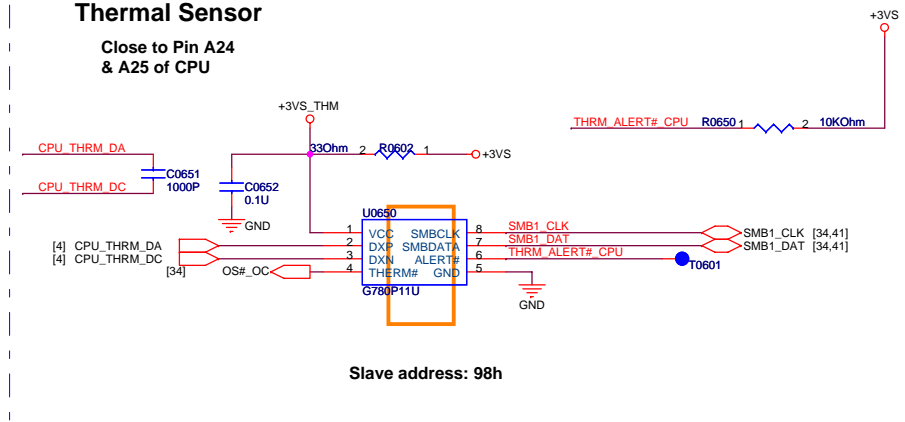
Follow DESIGN_IP M51Va



Cap Follow DesignIP
22U/6.3V 0805_55:11G235222625320



**Close to Pin A24
& A25 of CPU**



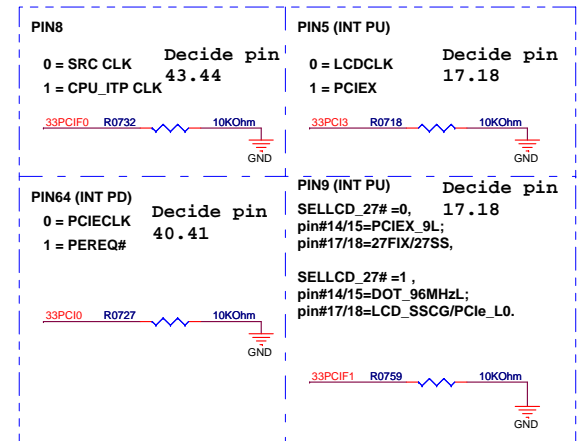
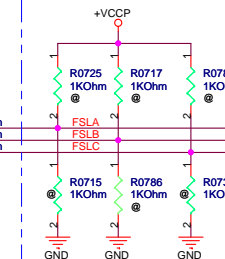
PEREQ#3
Byte15-bit 1/0 => PCIE_X4/2
(ICH,NEWCARD)

PEREQ#4
Byte15-bit 7/6/5 => PCIE_X7/5/3
(3GPLL,LAN,WLAN)

<Variant Name>

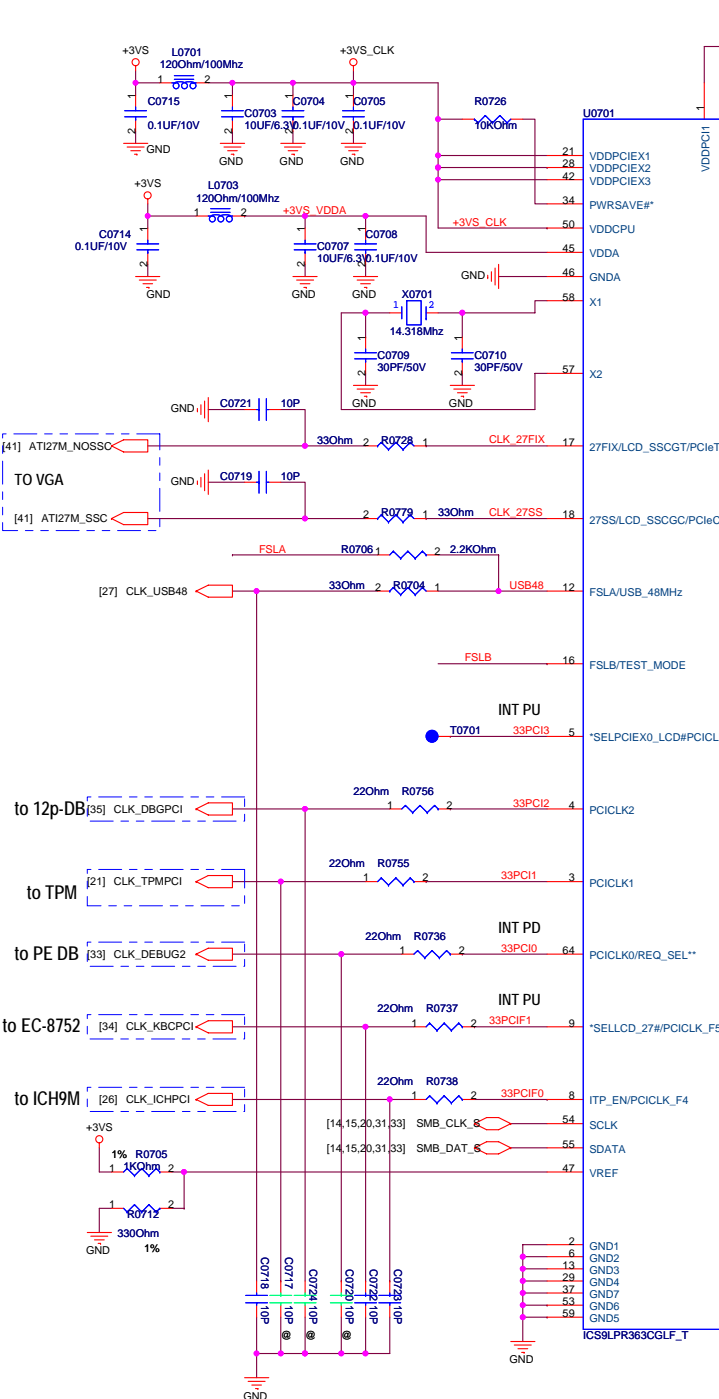
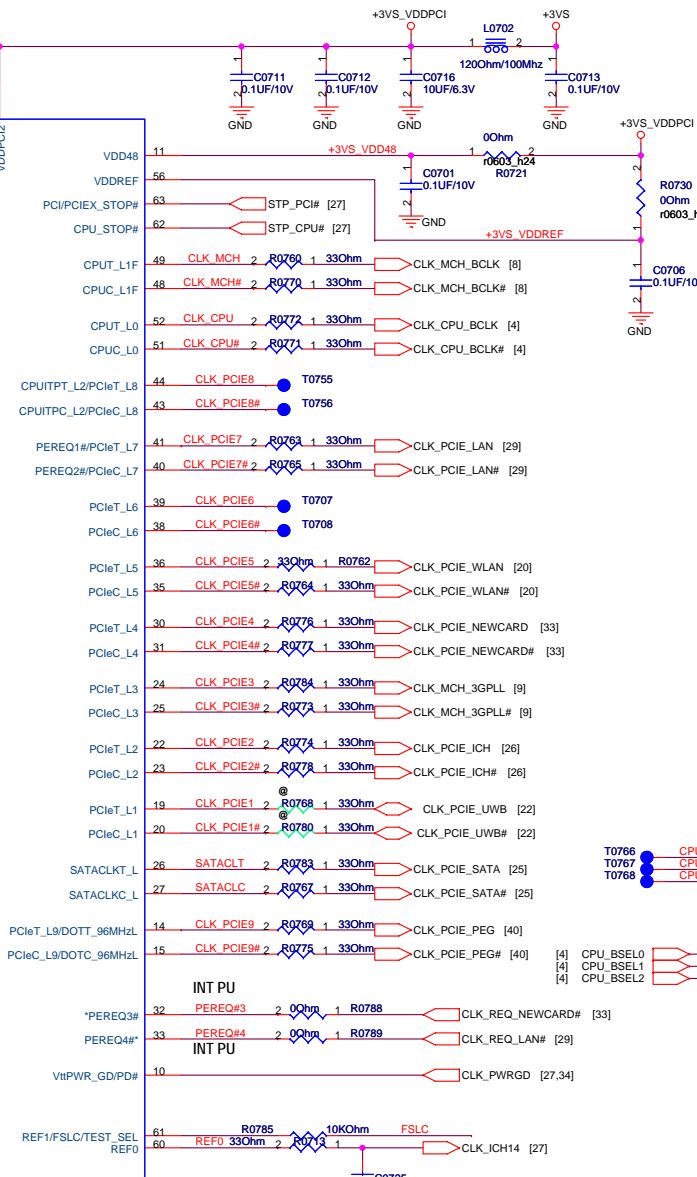
		FSLC	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

Default CPU Driven



T0766 CPU_BSEL0
T0767 CPU_BSEL1
T0768 CPU_BSEL2

[4] CPU_BSEL0 R0766 00Ohm 2 MCH_BSEL0 [9]
[4] CPU_BSEL1 R0733 00Ohm 2 MCH_BSEL1 [9]
[4] CPU_BSEL2 R0734 00Ohm 2 MCH_BSEL2 [9]



TO VGA

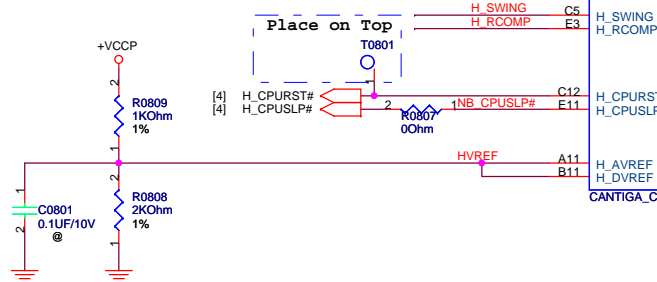
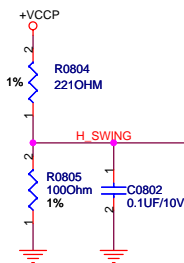
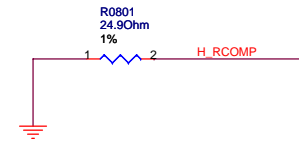
to 12p-DB

to TPM

to PE DB

to EC-8752

to ICH9M



U0801A					
H_D#0	F2	H_D#_0		H_A#_3	A14
H_D#1	G8	H_D#_1		H_A#_4	C15
H_D#2	F8	H_D#_2		H_A#_5	F16
H_D#3	E6	H_D#_3		H_A#_6	H13
H_D#4	G2	H_D#_4		H_A#_7	M16
H_D#5	H6	H_D#_5		H_A#_8	J13
H_D#6	H2	H_D#_6		H_A#_9	P16
H_D#7	F6	H_D#_7		H_A#_10	R16
H_D#8	D4	H_D#_8		H_A#_11	N17
H_D#9	H3	H_D#_9		H_A#_12	M13
H_D#10	M9	H_D#_10		H_A#_13	E17
H_D#11	M11	H_D#_11		H_A#_14	P17
H_D#12	J1	H_D#_12		H_A#_15	F17
H_D#13	J2	H_D#_13		H_A#_16	G20
H_D#14	N12	H_D#_14		H_A#_17	B19
H_D#15	J6	H_D#_15		H_A#_18	E20
H_D#16	L2	H_D#_16		H_A#_19	H16
H_D#17	R2	H_D#_17		H_A#_20	J20
H_D#18	N9	H_D#_18		H_A#_21	L17
H_D#19	L6	H_D#_19		H_A#_22	A17
H_D#20	M5	H_D#_20		H_A#_23	B17
H_D#21	J3	H_D#_21		H_A#_24	L16
H_D#22	N2	H_D#_22		H_A#_25	C21
H_D#23	R1	H_D#_23		H_A#_26	J17
H_D#24	N5	H_D#_24		H_A#_27	H16
H_D#25	N6	H_D#_25		H_A#_28	H20
H_D#26	P13	H_D#_26		H_A#_29	B18
H_D#27	N8	H_D#_27		H_A#_30	K17
H_D#28	L7	H_D#_28		H_A#_31	B20
H_D#29	N10	H_D#_29		H_A#_32	F21
H_D#30	M3	H_D#_30		H_A#_33	K21
H_D#31	Y3	H_D#_31		H_A#_34	L20
H_D#32	AD14	H_D#_32		H_A#_35	
H_D#33	Y6	H_D#_33			
H_D#34	Y10	H_D#_34			
H_D#35	Y12	H_D#_35			
H_D#36	Y14	H_D#_36			
H_D#37	Y7	H_D#_37			
H_D#38	W2	H_D#_38			
H_D#39	AA8	H_D#_39			
H_D#40	Y9	H_D#_40			
H_D#41	AA13	H_D#_41			
H_D#42	AA9	H_D#_42			
H_D#43	AA11	H_D#_43			
H_D#44	AD11	H_D#_44			
H_D#45	AD10	H_D#_45			
H_D#46	AD13	H_D#_46			
H_D#47	AE12	H_D#_47			
H_D#48	AE9	H_D#_48			
H_D#49	AA2	H_D#_49			
H_D#50	AD8	H_D#_50			
H_D#51	AA3	H_D#_51			
H_D#52	AD3	H_D#_52			
H_D#53	AD7	H_D#_53			
H_D#54	AE14	H_D#_54			
H_D#55	AE3	H_D#_55			
H_D#56	AC1	H_D#_56			
H_D#57	AE3	H_D#_57			
H_D#58	AC3	H_D#_58			
H_D#59	AE11	H_D#_59			
H_D#60	AE8	H_D#_60			
H_D#61	AE2	H_D#_61			
H_D#62	AD6	H_D#_62			
H_D#63		H_D#_63			

HOST

[4] H_A#[35:3] H_A#[35:3]

[4] H_REQ#[4:0] H_REQ#[4:0]

[4] H_D#[63:0] H_D#[63:0]

CLK_MCH_BCLK [7] CLK_MCH_BCLK# [7]

H_ADS# H12 H_ADS# [4]
H_ADSTB#_0 B16 H_ADSTB#0 [4]
H_ADSTB#_1 G17 H_ADSTB#1 [4]
H_BNR# A9 H_BNR# [4]
H_BPRI# E11 H_BPRI# [4]
H_BRQ# G12 H_BRQ# [4]
H_DEFER# E9 H_DEFER# [4]
H_DBSY# B10 H_DBSY# [4]
HPLL_CLK AH7
HPLL_CLK# AH6
H_DPWR# J11 H_DPWR# [4]
H_DRDY# F9 H_DRDY# [4]
H_HIT# H8 H_HIT# [4]
H_HITM# E12 H_HITM# [4]
H_LOCK# H11 H_LOCK# [4]
H_TRDY# C9 H_TRDY# [4]

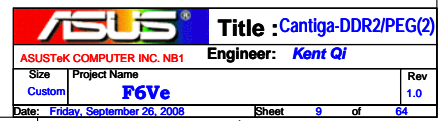
H_DINV#_0 J8 H_DINV#0 [4]
H_DINV#_1 I3 H_DINV#1 [4]
H_DINV#_2 Y13 H_DINV#2 [4]
H_DINV#_3 Y1 H_DINV#3 [4]

H_DSTBN#_0 L10 H_DSTBN#0 [4]
H_DSTBN#_1 M7 H_DSTBN#1 [4]
H_DSTBN#_2 AA5 H_DSTBN#2 [4]
H_DSTBN#_3 AE6 H_DSTBN#3 [4]

H_DSTBP#_0 L9 H_DSTBP#0 [4]
H_DSTBP#_1 M8 H_DSTBP#1 [4]
H_DSTBP#_2 AA6 H_DSTBP#2 [4]
H_DSTBP#_3 AE5 H_DSTBP#3 [4]

H_REQ#_0 B15 H_REQ#0
H_REQ#_1 K13 H_REQ#1
H_REQ#_2 F13 H_REQ#2
H_REQ#_3 B13 H_REQ#3
H_REQ#_4 B14 H_REQ#4

H_RS#_0 B6 H_RS#0 [4]
H_RS#_1 F12 H_RS#1 [4]
H_RS#_2 C8 H_RS#2 [4]



[14] M_A_DQ[0:63]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AN38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AJ40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AU44	SA_DQ_14
M A DQ15	AU42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BA41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AV37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BA38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	BD33	SA_DQ_31
M A DQ32	AU11	SA_DQ_32
M A DQ33	BC11	SA_DQ_33
M A DQ34	BA12	SA_DQ_34
M A DQ35	AU13	SA_DQ_35
M A DQ36	AV13	SA_DQ_36
M A DQ37	BD12	SA_DQ_37
M A DQ38	BC12	SA_DQ_38
M A DQ39	BA9	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AU10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AY8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AU5	SA_DQ_52
M A DQ53	AU6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0 [14,16]
SA_BS_1	BG18	M_A_BS1 [14,16]
SA_BS_2	AT25	M_A_BS2 [14,16]
SA_RAS#	BB20	M_A_RAS# [14,16]
SA_CAS#	BD20	M_A_CAS# [14,16]
SA_WE#	AY20	M_A_WE# [14,16]

SA_DM_0	AM37	M_A_DM0	M_A_DM[0:7] [14]
SA_DM_1	AT41	M_A_DM1	
SA_DM_2	AY41	M_A_DM2	
SA_DM_3	AU39	M_A_DM3	
SA_DM_4	BB12	M_A_DM4	
SA_DM_5	AY6	M_A_DM5	
SA_DM_6	AT7	M_A_DM6	
SA_DM_7	AJ5	M_A_DM7	

SA_DQS_0	AJ44	M_A_DQS0	M_A_DQS[0:7] [14]
SA_DQS_1	AT44	M_A_DQS1	
SA_DQS_2	BA43	M_A_DQS2	
SA_DQS_3	BC37	M_A_DQS3	
SA_DQS_4	AW12	M_A_DQS4	
SA_DQS_5	BC8	M_A_DQS5	
SA_DQS_6	AU8	M_A_DQS6	
SA_DQS_7	AM7	M_A_DQS7	
SA_DQS#_0	AJ43	M_A_DQS#0	M_A_DQS#[0:7] [14]
SA_DQS#_1	AT43	M_A_DQS#1	
SA_DQS#_2	BA44	M_A_DQS#2	
SA_DQS#_3	BD37	M_A_DQS#3	
SA_DQS#_4	AY12	M_A_DQS#4	
SA_DQS#_5	BD8	M_A_DQS#5	
SA_DQS#_6	AU9	M_A_DQS#6	
SA_DQS#_7	AM8	M_A_DQS#7	

SA_MA_0	BA21	M_A_A0	M_A_A[0:14] [14,16]
SA_MA_1	BC24	M_A_A1	
SA_MA_2	BG24	M_A_A2	
SA_MA_3	BH24	M_A_A3	
SA_MA_4	BG25	M_A_A4	
SA_MA_5	BA24	M_A_A5	
SA_MA_6	BD24	M_A_A6	
SA_MA_7	BG27	M_A_A7	
SA_MA_8	BF25	M_A_A8	
SA_MA_9	AW24	M_A_A9	
SA_MA_10	BC21	M_A_A10	
SA_MA_11	BG26	M_A_A11	
SA_MA_12	BH26	M_A_A12	
SA_MA_13	BH17	M_A_A13	
SA_MA_14	AY25	M_A_A14	

[15] M_B_DQ[0:63]

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AU47	SB_DQ_8
M B DQ9	EA48	SB_DQ_9
M B DQ10	EA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT47	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BE11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BG7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY1	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AU3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AJ1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0 [15,16]
SB_BS_1	BB17	M_B_BS1 [15,16]
SB_BS_2	BB33	M_B_BS2 [15,16]
SB_RAS#	AU17	M_B_RAS# [15,16]
SB_CAS#	BG16	M_B_CAS# [15,16]
SB_WE#	BF14	M_B_WE# [15,16]

SB_DM_0	AM47	M_B_DM0	M_B_DM[0:7] [15]
SB_DM_1	AY47	M_B_DM1	
SB_DM_2	BD40	M_B_DM2	
SB_DM_3	BF35	M_B_DM3	
SB_DM_4	BG11	M_B_DM4	
SB_DM_5	BA3	M_B_DM5	
SB_DM_6	AP1	M_B_DM6	
SB_DM_7	AK2	M_B_DM7	

SB_DQS_0	AL47	M_B_DQS0	M_B_DQS[0:7] [15]
SB_DQS_1	AV48	M_B_DQS1	
SB_DQS_2	BG41	M_B_DQS2	
SB_DQS_3	BH9	M_B_DQS3	
SB_DQS_4	BB2	M_B_DQS4	
SB_DQS_5	BB2	M_B_DQS5	
SB_DQS_6	AU1	M_B_DQS6	
SB_DQS_7	AN6	M_B_DQS7	
SB_DQS#_0	AL46	M_B_DQS#0	M_B_DQS#[0:7] [15]
SB_DQS#_1	AV47	M_B_DQS#1	
SB_DQS#_2	BH41	M_B_DQS#2	
SB_DQS#_3	BH37	M_B_DQS#3	
SB_DQS#_4	BG9	M_B_DQS#4	
SB_DQS#_5	BC2	M_B_DQS#5	
SB_DQS#_6	AT2	M_B_DQS#6	
SB_DQS#_7	AN5	M_B_DQS#7	

SB_MA_0	AV17	M_B_A0	M_B_A[0:14] [15,16]
SB_MA_1	BA25	M_B_A1	
SB_MA_2	BC25	M_B_A2	
SB_MA_3	AU25	M_B_A3	
SB_MA_4	AW25	M_B_A4	
SB_MA_5	BB28	M_B_A5	
SB_MA_6	AU28	M_B_A6	
SB_MA_7	AW28	M_B_A7	
SB_MA_8	AT33	M_B_A8	
SB_MA_9	BD33	M_B_A9	
SB_MA_10	BB16	M_B_A10	
SB_MA_11	AW33	M_B_A11	
SB_MA_12	AY33	M_B_A12	
SB_MA_13	BH15	M_B_A13	
SB_MA_14	AU33	M_B_A14	

2.6A for DDR2 667
3A for DDR2 800

Confirm by Intel
TINNA Confirm.

Need to check

Route VCC_AXG_SENSE and
VSS_AXG_SENSE differentially.

U0801G

VCC SM

VCC GFX NCTF

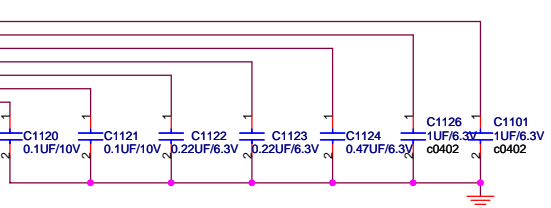
VCC GFX

VCC SM LF

- VCC_AXG_NCTF_1
- VCC_AXG_NCTF_2
- VCC_AXG_NCTF_3
- VCC_AXG_NCTF_4
- VCC_AXG_NCTF_5
- VCC_AXG_NCTF_6
- VCC_AXG_NCTF_7
- VCC_AXG_NCTF_8
- VCC_AXG_NCTF_9
- VCC_AXG_NCTF_10
- VCC_AXG_NCTF_11
- VCC_AXG_NCTF_12
- VCC_AXG_NCTF_13
- VCC_AXG_NCTF_14
- VCC_AXG_NCTF_15
- VCC_AXG_NCTF_16
- VCC_AXG_NCTF_17
- VCC_AXG_NCTF_18
- VCC_AXG_NCTF_19
- VCC_AXG_NCTF_20
- VCC_AXG_NCTF_21
- VCC_AXG_NCTF_22
- VCC_AXG_NCTF_23
- VCC_AXG_NCTF_24
- VCC_AXG_NCTF_25
- VCC_AXG_NCTF_26
- VCC_AXG_NCTF_27
- VCC_AXG_NCTF_28
- VCC_AXG_NCTF_29
- VCC_AXG_NCTF_30
- VCC_AXG_NCTF_31
- VCC_AXG_NCTF_32
- VCC_AXG_NCTF_33
- VCC_AXG_NCTF_34
- VCC_AXG_NCTF_35
- VCC_AXG_NCTF_36
- VCC_AXG_NCTF_37
- VCC_AXG_NCTF_38
- VCC_AXG_NCTF_39
- VCC_AXG_NCTF_40
- VCC_AXG_NCTF_41
- VCC_AXG_NCTF_42
- VCC_AXG_NCTF_43
- VCC_AXG_NCTF_44
- VCC_AXG_NCTF_45
- VCC_AXG_NCTF_46
- VCC_AXG_NCTF_47
- VCC_AXG_NCTF_48
- VCC_AXG_NCTF_49
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- VCC_AXG_NCTF_54
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- VCC_AXG_NCTF_60

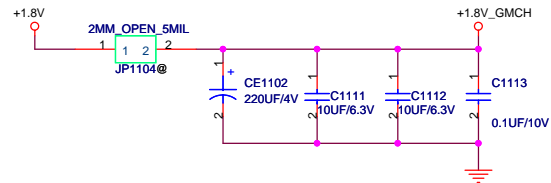
- W28
- W28
- W26
- W26
- W25
- W25
- W24
- W24
- W23
- W23
- V23
- AM21
- AL21
- AK21
- W21
- V21
- U21
- AM20
- AK20
- W20
- U20
- AL19
- AK19
- AJ19
- AH19
- AF19
- AE19
- AB19
- AA19
- Y19
- W19
- V19
- U19
- AM17
- AK17
- AJ17
- AH17
- AG17
- AE17
- AB17
- AA17
- Y17
- W17
- V17
- U17
- AM16
- AK16
- AJ16
- AH16
- AG16
- AE16
- AB16
- AA16
- Y16
- W16
- V16
- U16

- VCC_SM_LF1
- VCC_SM_LF2
- VCC_SM_LF3
- VCC_SM_LF4
- VCC_SM_LF5
- VCC_SM_LF6
- VCC_SM_LF7



2.178A (W ME)
1.67A (W/O ME)

2.6A for DDR2 667
3A for DDR2 800



U0801F

VCC CORE

VCC NCTF

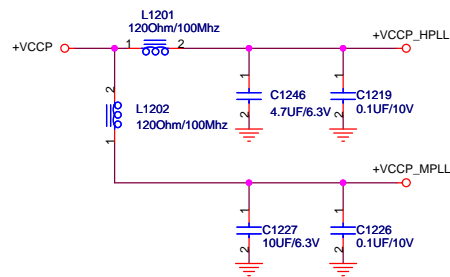
VCC NCTF

- VCC_1
- VCC_2
- VCC_3
- VCC_4
- VCC_5
- VCC_6
- VCC_7
- VCC_8
- VCC_9
- VCC_10
- VCC_11
- VCC_12
- VCC_13
- VCC_14
- VCC_15
- VCC_16
- VCC_17
- VCC_18
- VCC_19
- VCC_20
- VCC_21
- VCC_22
- VCC_23
- VCC_24
- VCC_25
- VCC_26
- VCC_27
- VCC_28
- VCC_29
- VCC_30
- VCC_31
- VCC_32
- VCC_33
- VCC_34
- VCC_35

- VCC_NCTF_1
- VCC_NCTF_2
- VCC_NCTF_3
- VCC_NCTF_4
- VCC_NCTF_5
- VCC_NCTF_6
- VCC_NCTF_7
- VCC_NCTF_8
- VCC_NCTF_9
- VCC_NCTF_10
- VCC_NCTF_11
- VCC_NCTF_12
- VCC_NCTF_13
- VCC_NCTF_14
- VCC_NCTF_15
- VCC_NCTF_16
- VCC_NCTF_17
- VCC_NCTF_18
- VCC_NCTF_19
- VCC_NCTF_20
- VCC_NCTF_21
- VCC_NCTF_22
- VCC_NCTF_23
- VCC_NCTF_24
- VCC_NCTF_25
- VCC_NCTF_26
- VCC_NCTF_27
- VCC_NCTF_28
- VCC_NCTF_29
- VCC_NCTF_30
- VCC_NCTF_31
- VCC_NCTF_32
- VCC_NCTF_33
- VCC_NCTF_34
- VCC_NCTF_35
- VCC_NCTF_36
- VCC_NCTF_37
- VCC_NCTF_38
- VCC_NCTF_39
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- VCC_NCTF_41
- VCC_NCTF_42
- VCC_NCTF_43
- VCC_NCTF_44

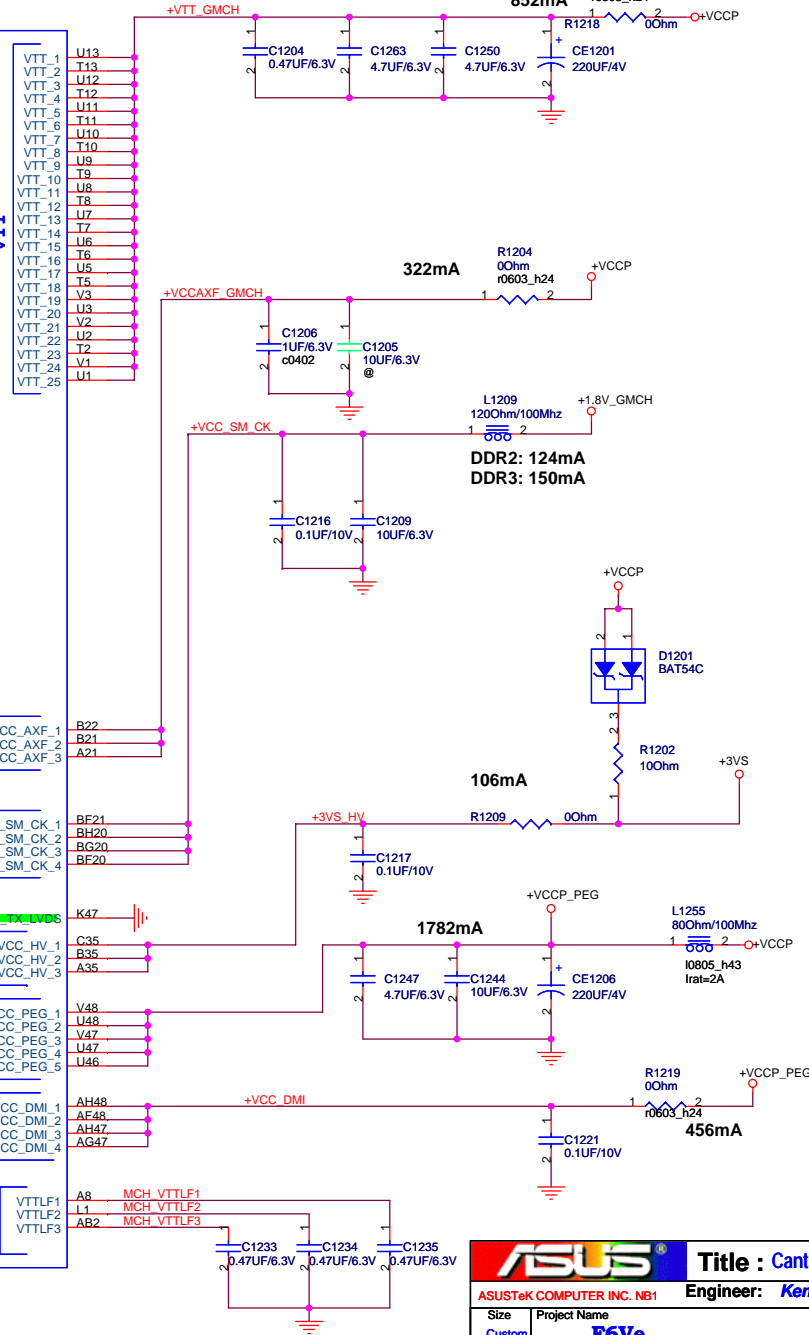
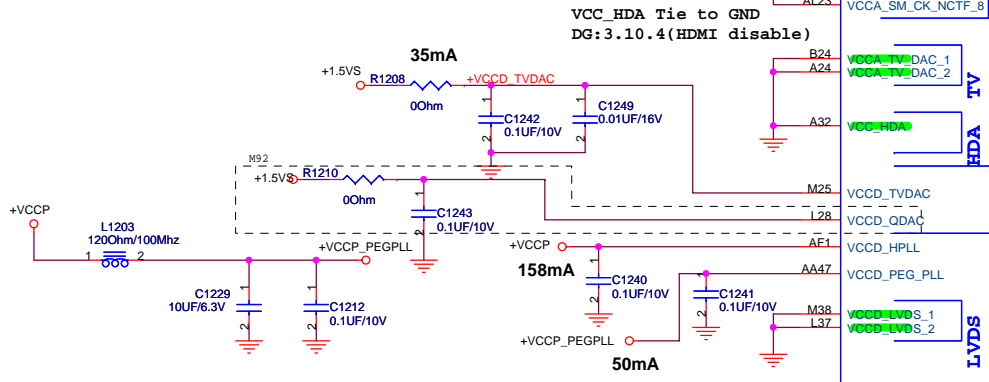
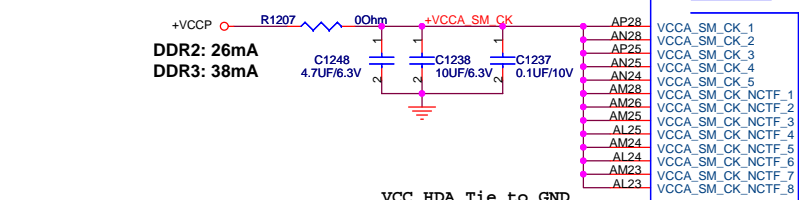
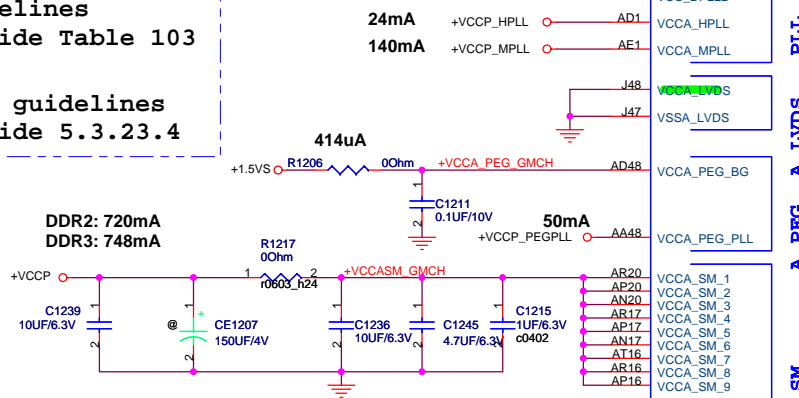
+VCC_GMCH

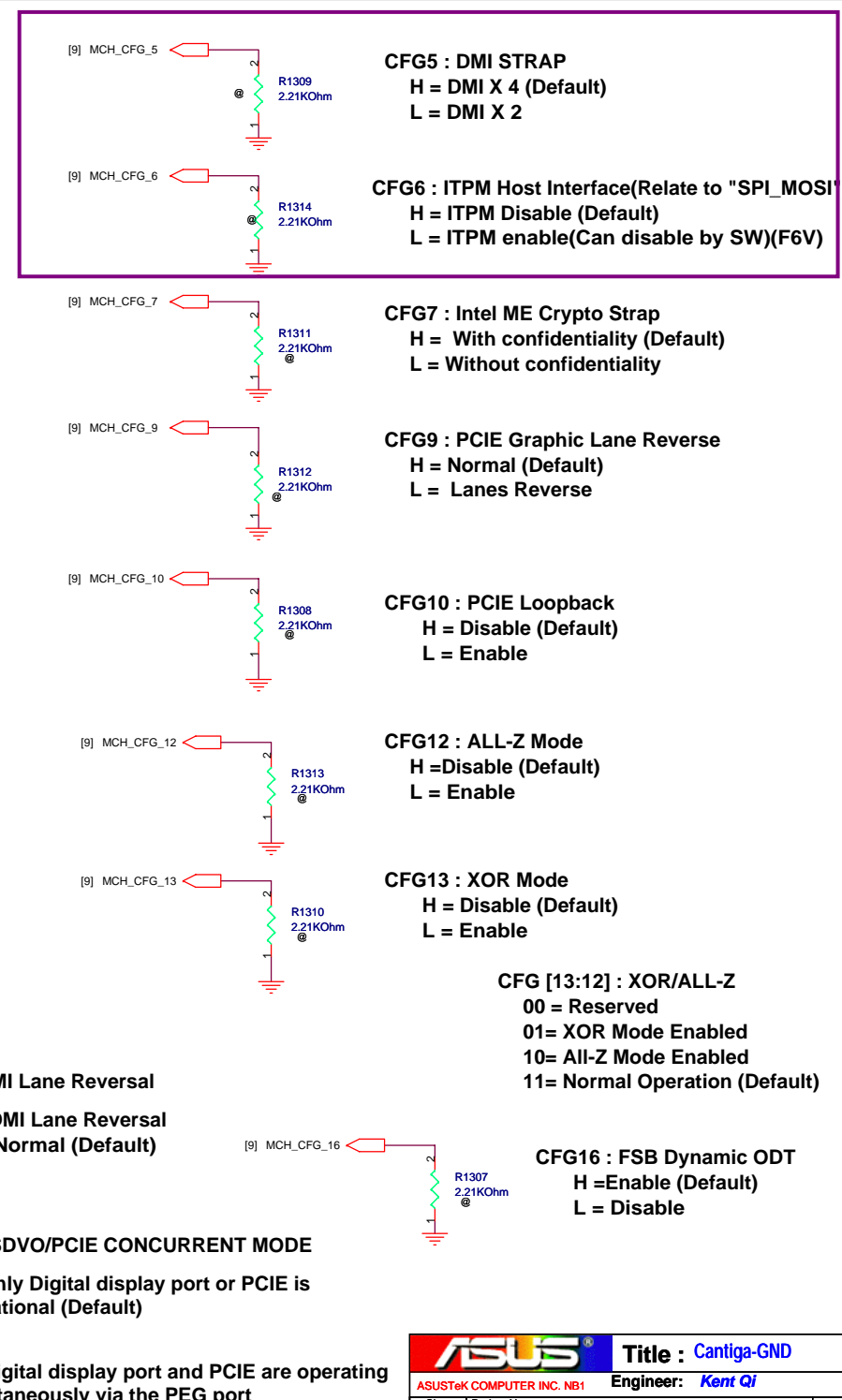
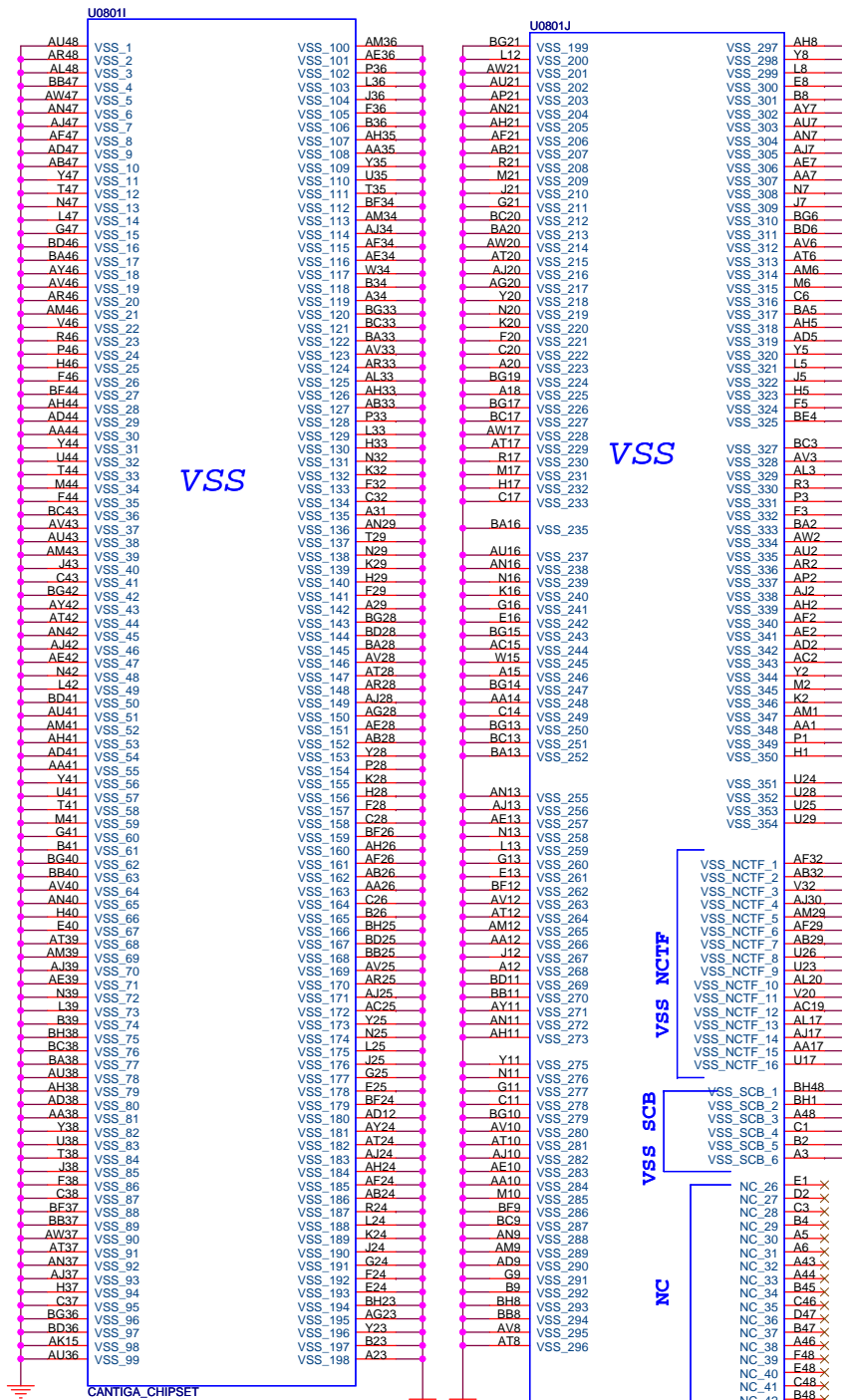
CANTIGA_CHIPSET

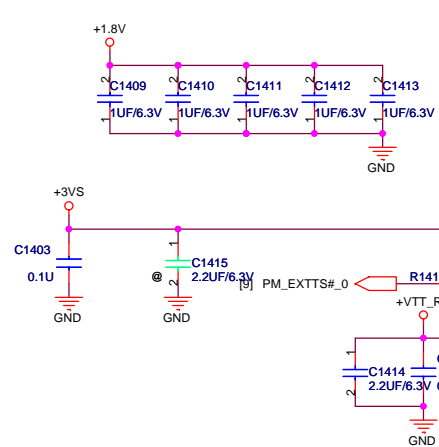
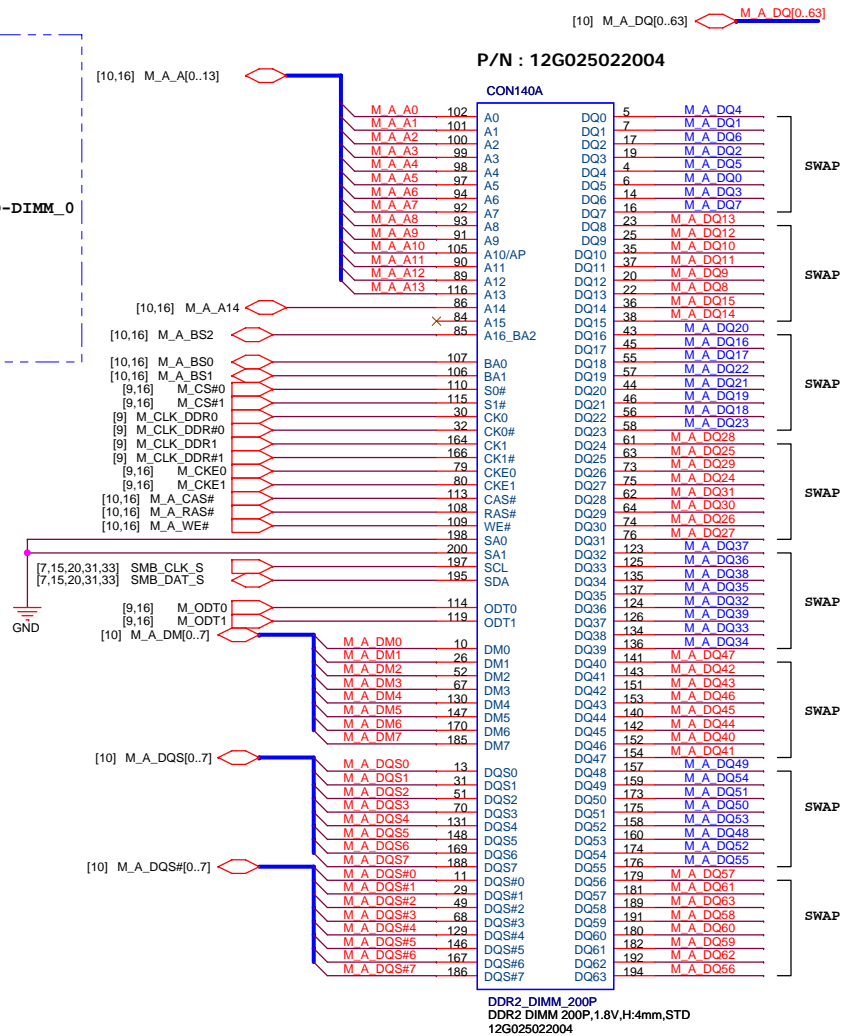
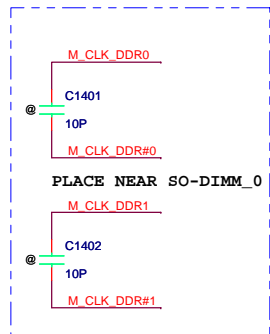


Power disable guidelines
Refer to Design Guide Table 103

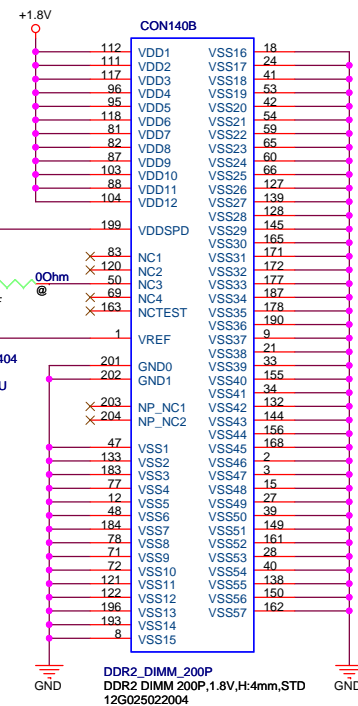
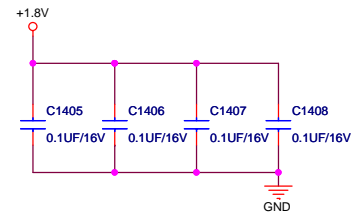
iAMT Power disable guidelines
Refer to Design Guide 5.3.23.4





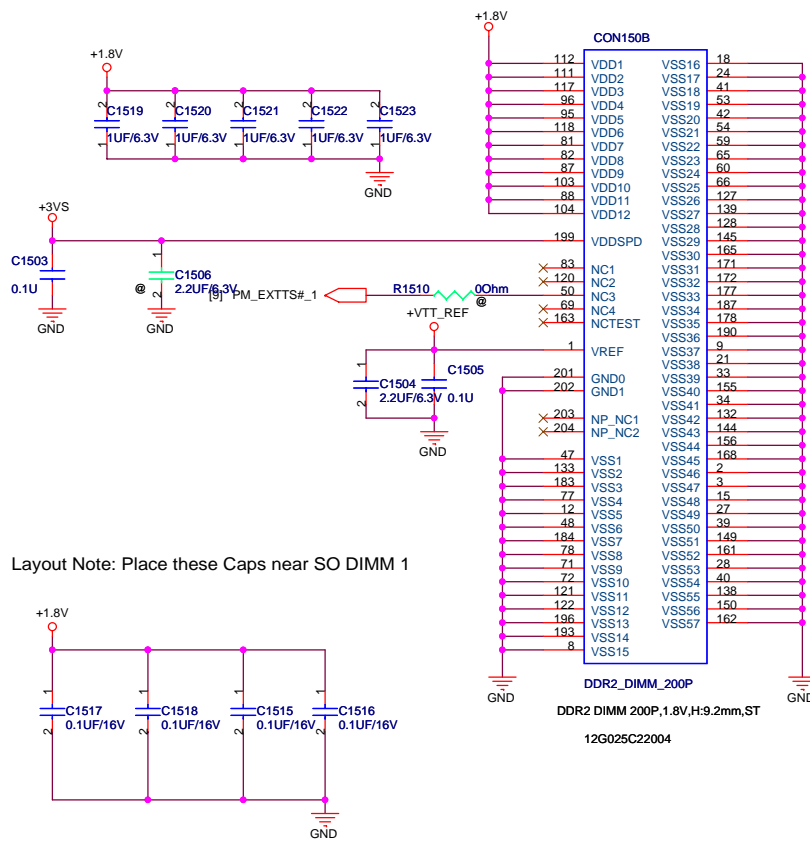
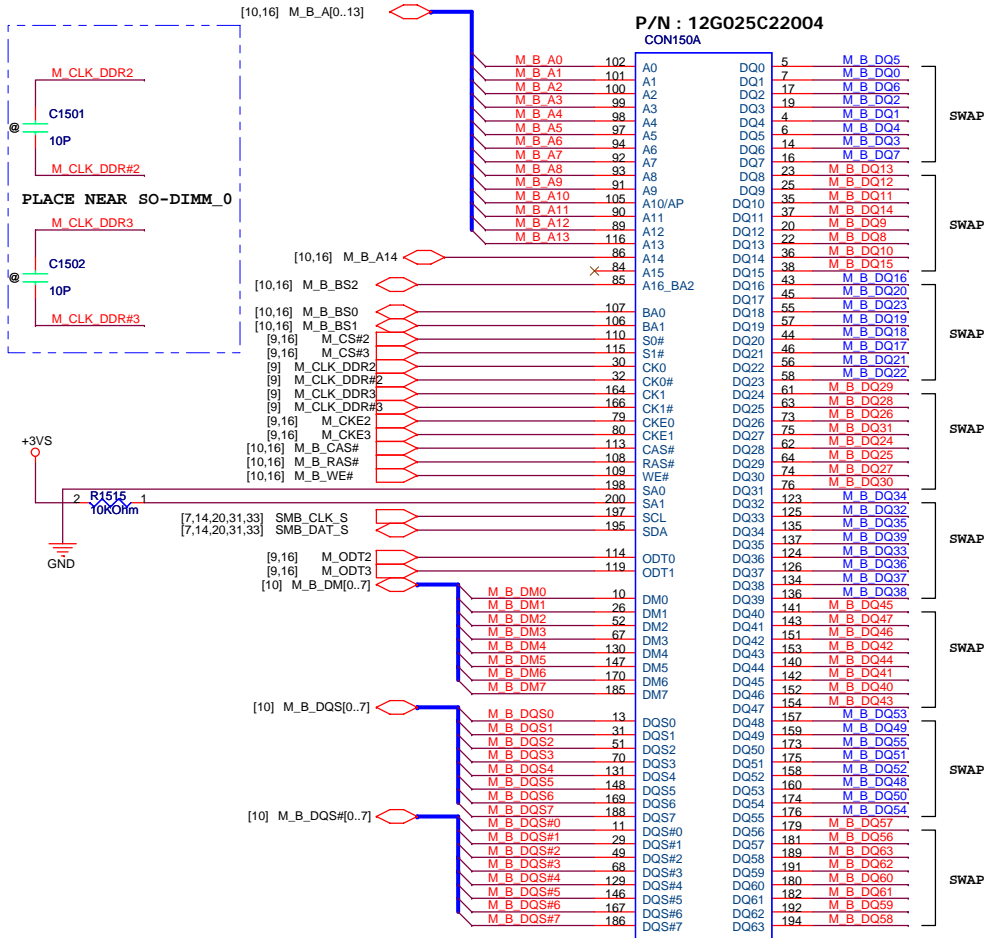


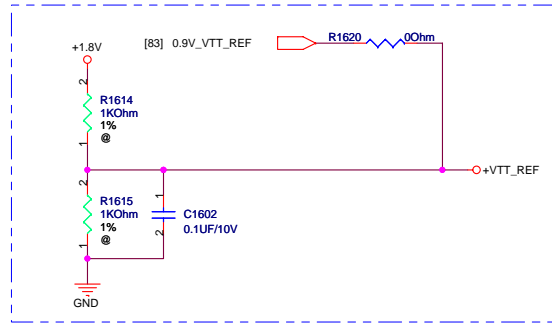
Layout Note: Place these Caps near SO DIMM 0



<Variant Name>

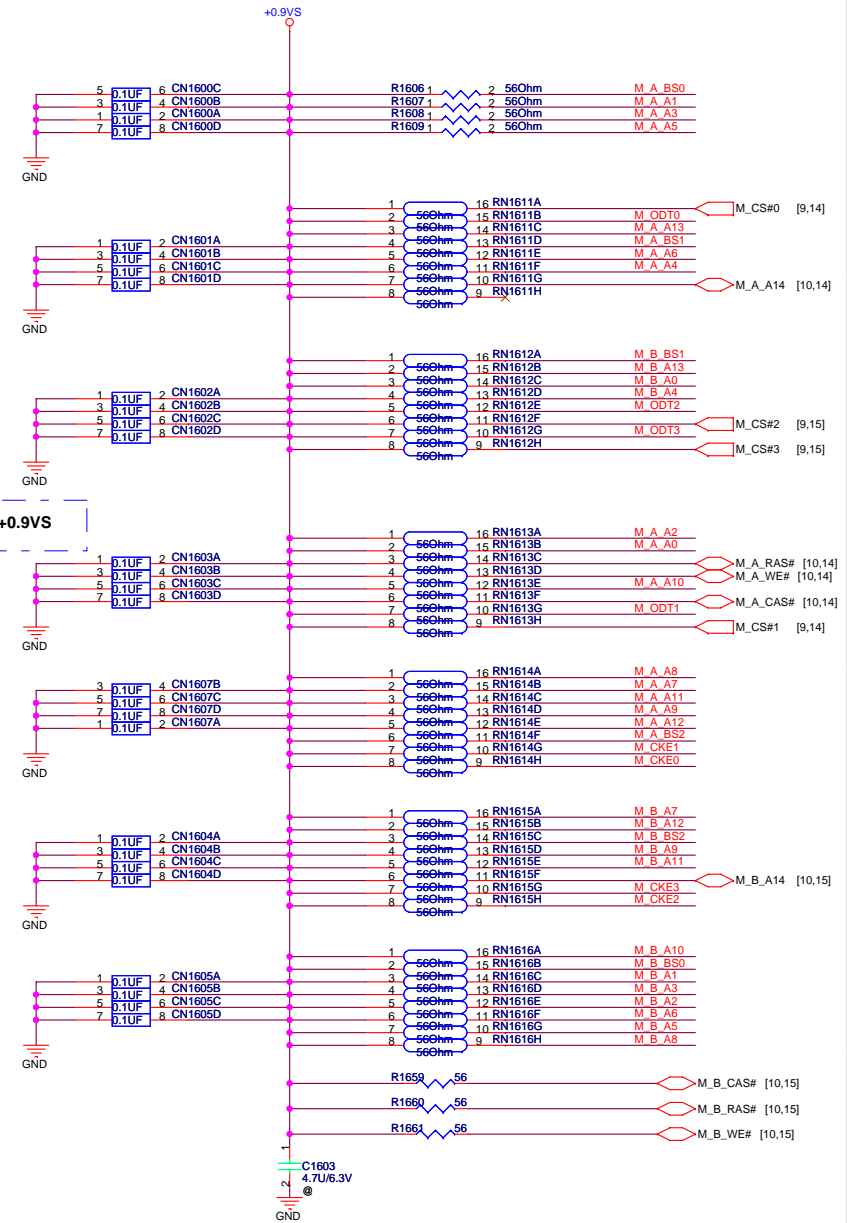
ASUS		Title : DDR2 SO-DIMM 0	
ASUSTeK COMPUTER INC		Engineer: Kent Qi	
Size	Project Name	Rev	
Custom	F6Ve	1.0	
Date: Friday, September 26, 2008	Sheet	14	of 64





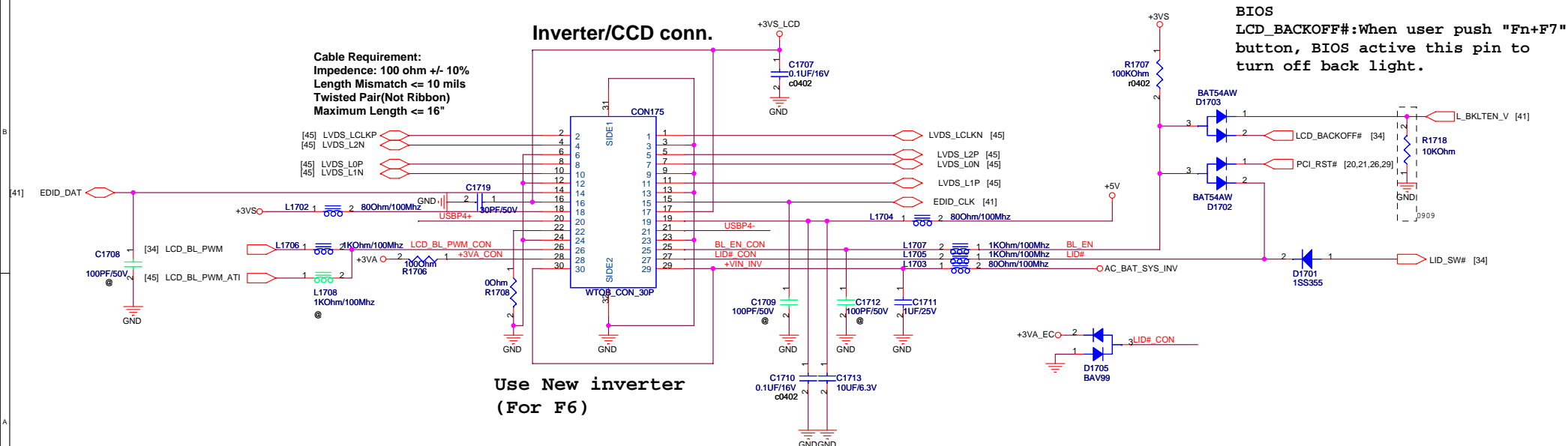
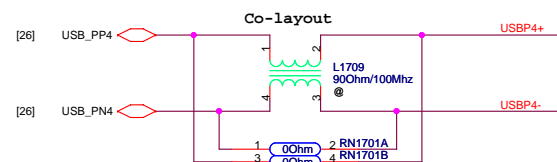
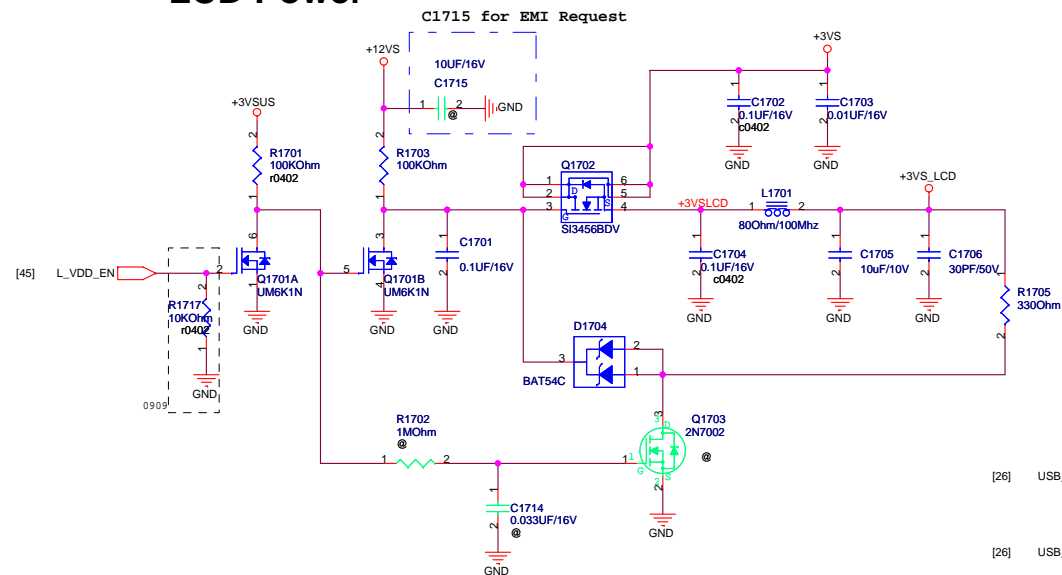
M_A_A[0..13] [10,14]
 M_A_BS[0..2] [10,14]
 M_B_A[0..13] [10,15]
 M_B_BS[0..2] [10,15]
 M_CKE[0..3] [9,14,15]
 M_ODT[0..3] [9,14,15]

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

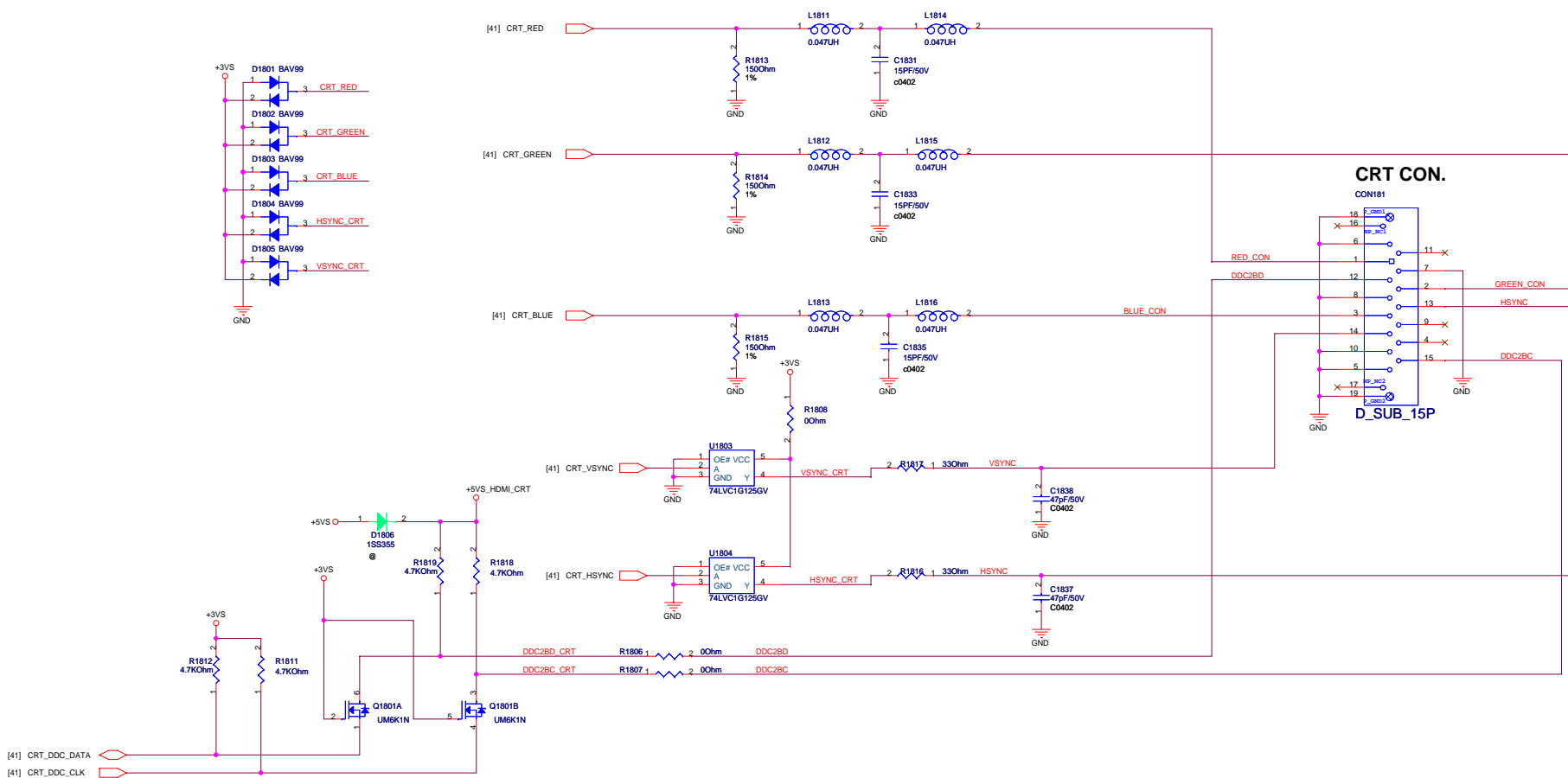


<Variant Name>

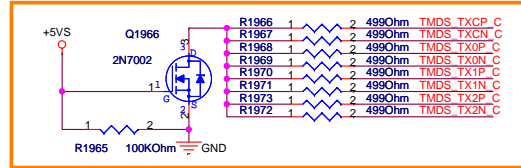
LCD Power



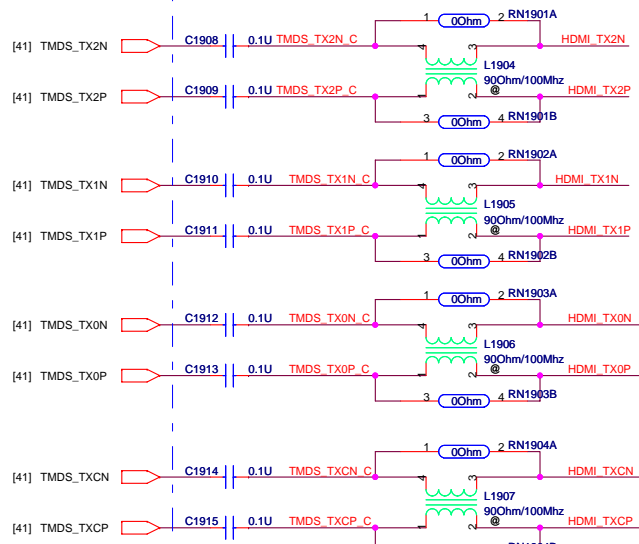
sualaptop365.edu.vn



Close to CONNECTOR

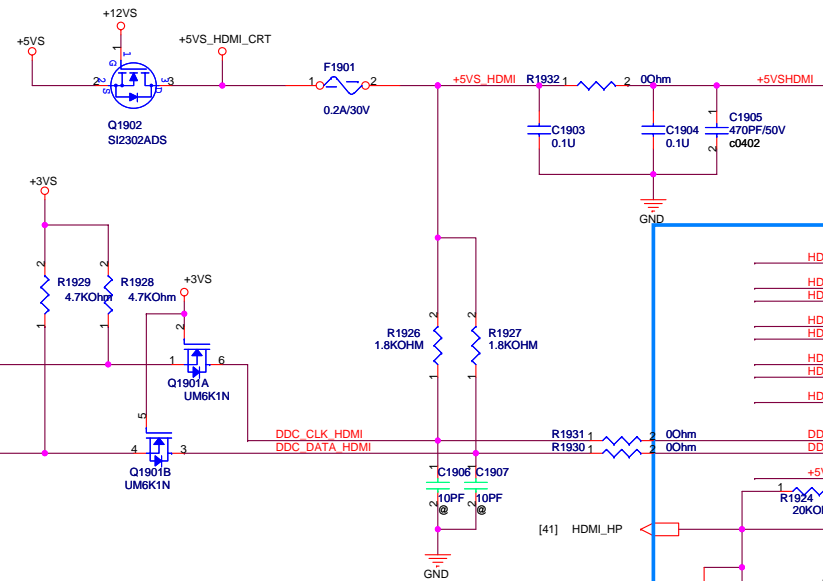


Close to CONNECTOR



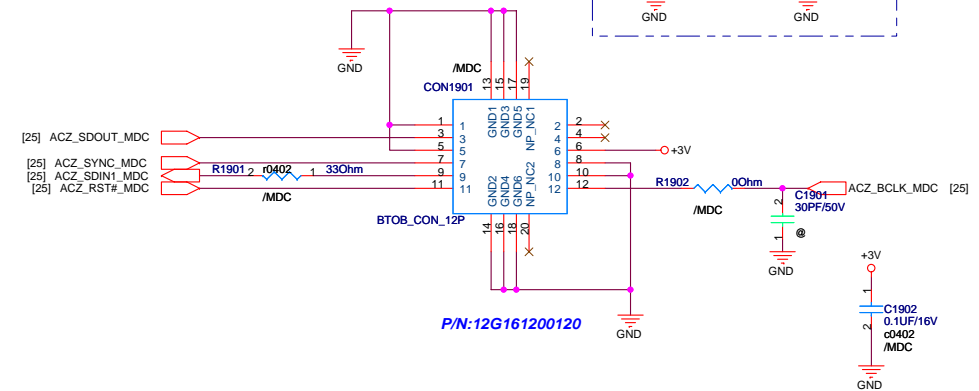
[41] HDMI_DDC_CLK

[41] HDMI_DDC_DATA

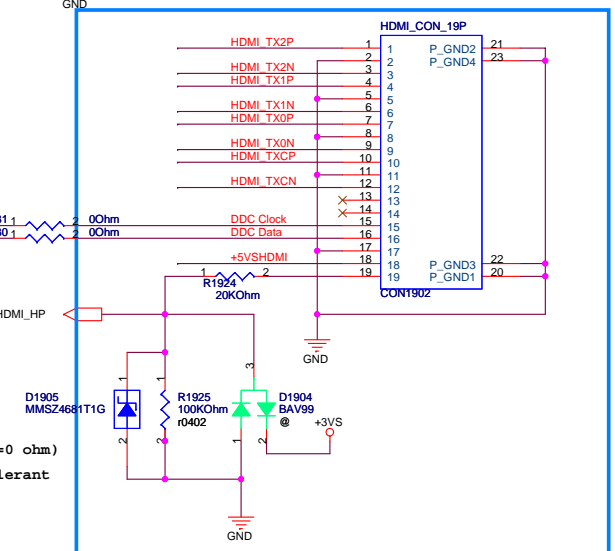


Note: 1. R1930,R1931,R1932: For EMI.(default=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +3V tolerant

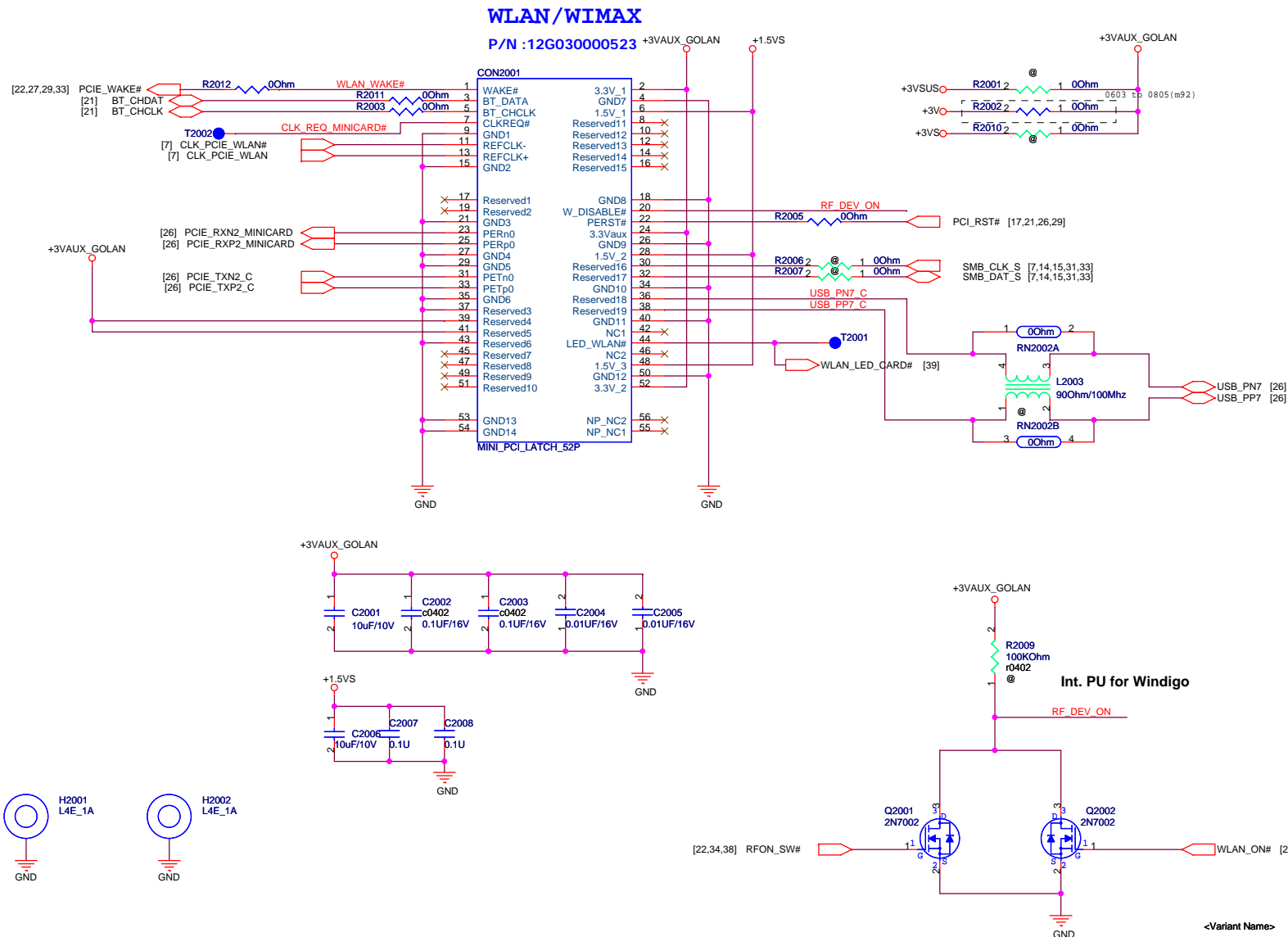
MDC CON.

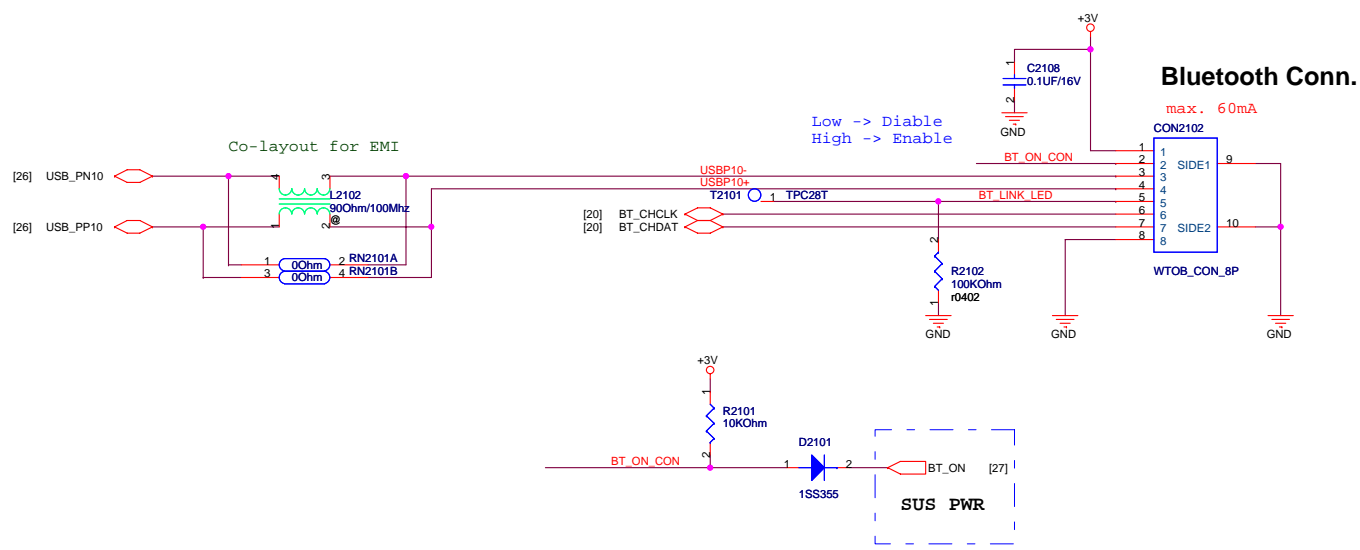


HDMI CON.

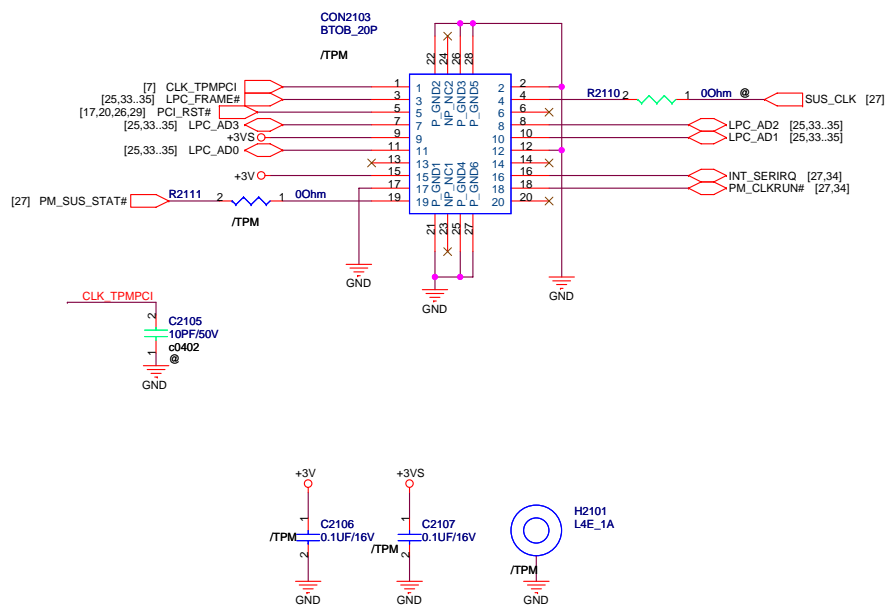


<Variant Name>



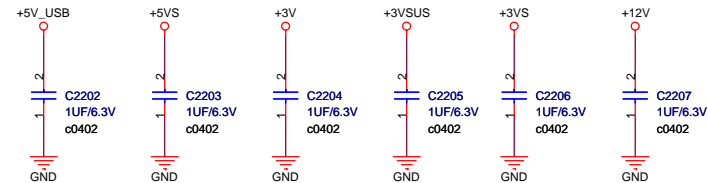
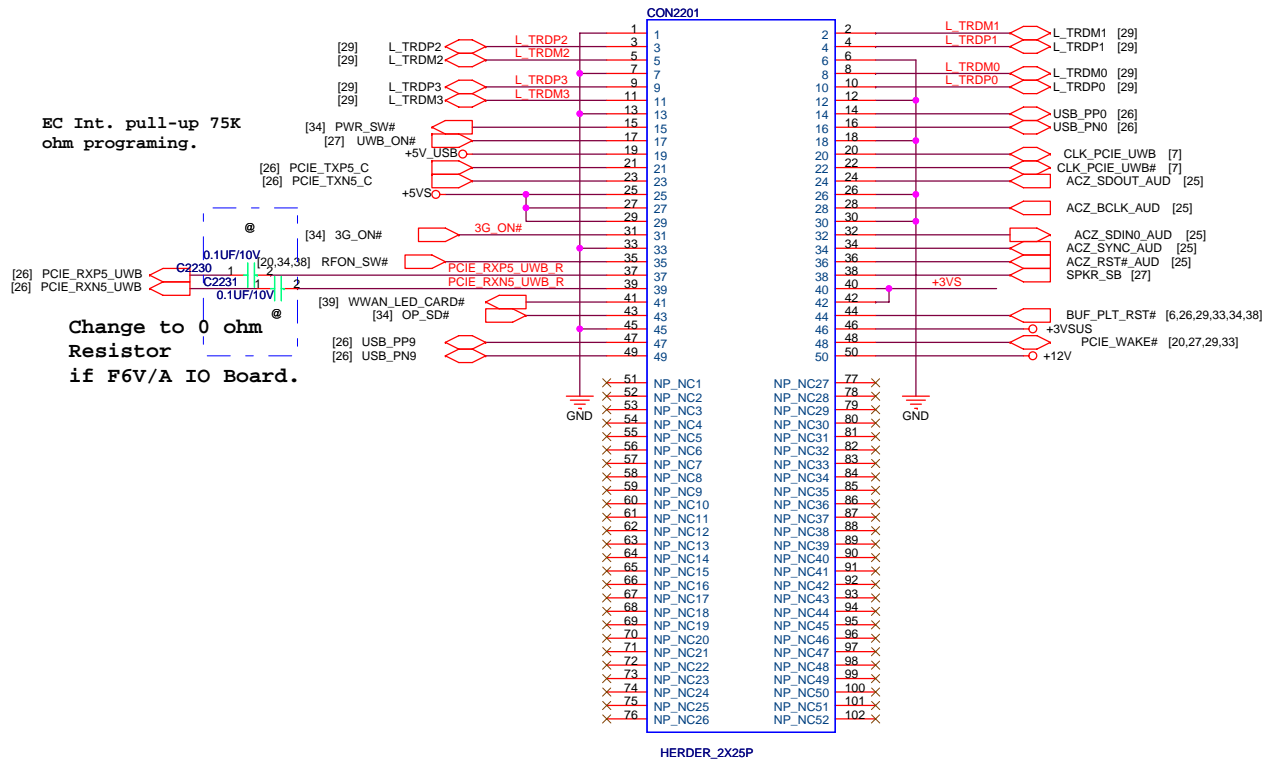


TPM Module Conn.



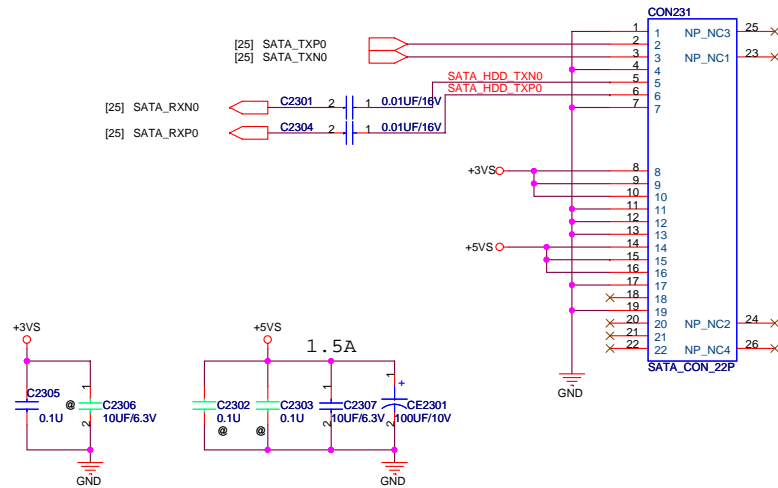
EC Int. pull-up 75K
ohm programing.

Change to 0 ohm
Resistor
if F6V/A IO Board.



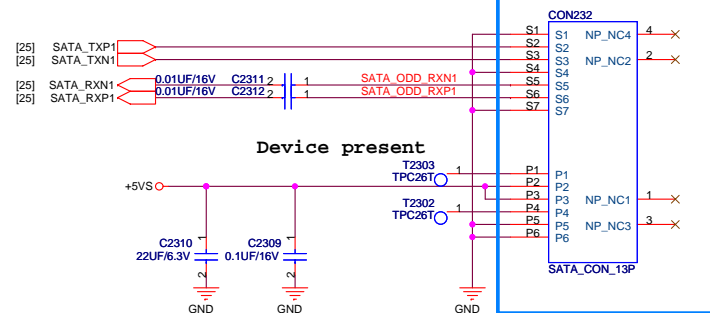
SATA HDD CON

12G15100022K

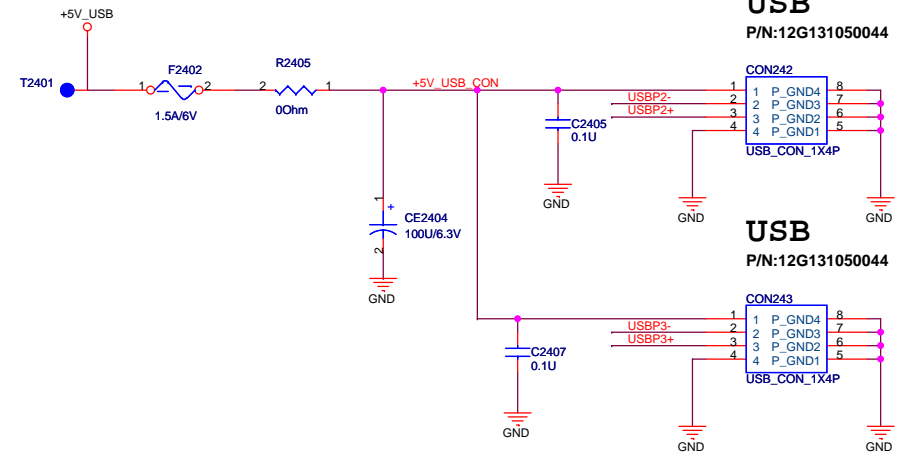
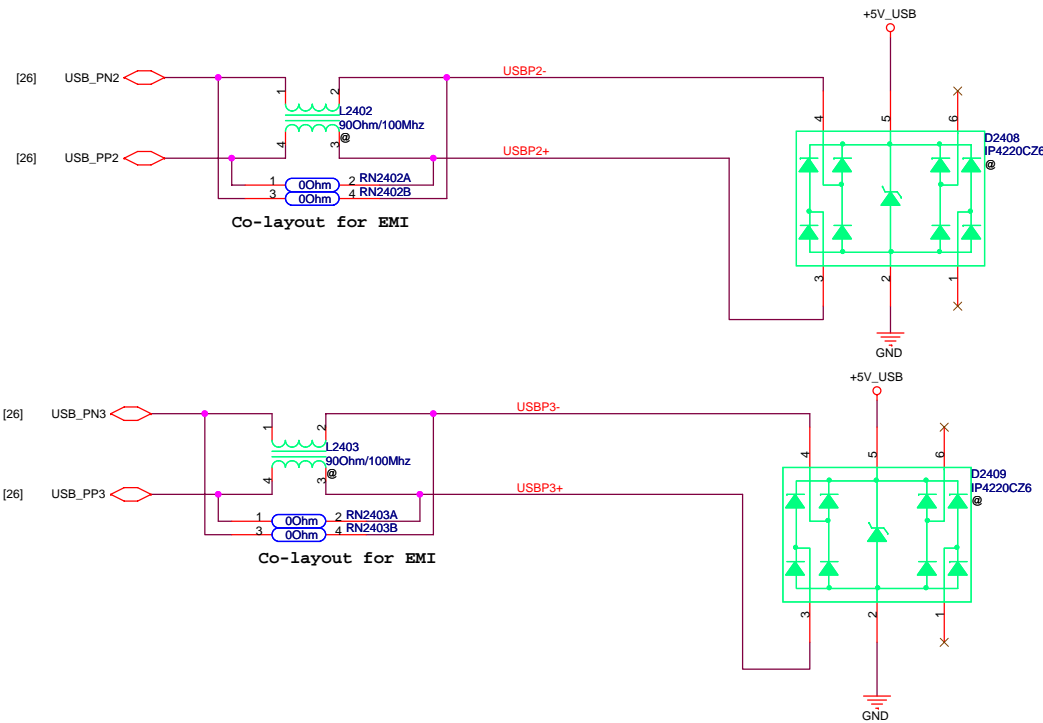
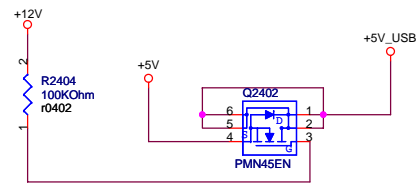


SATA ODD CON

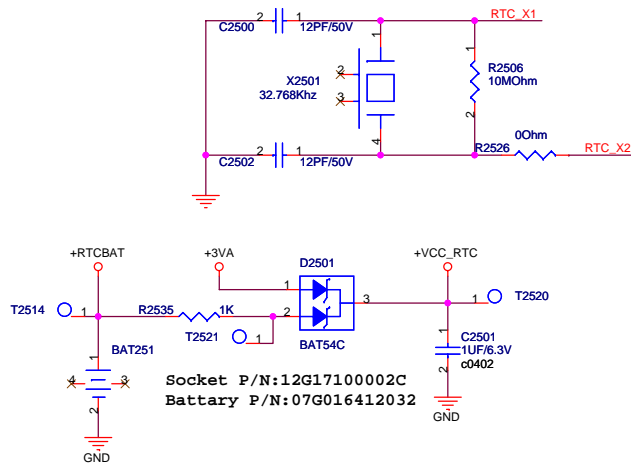
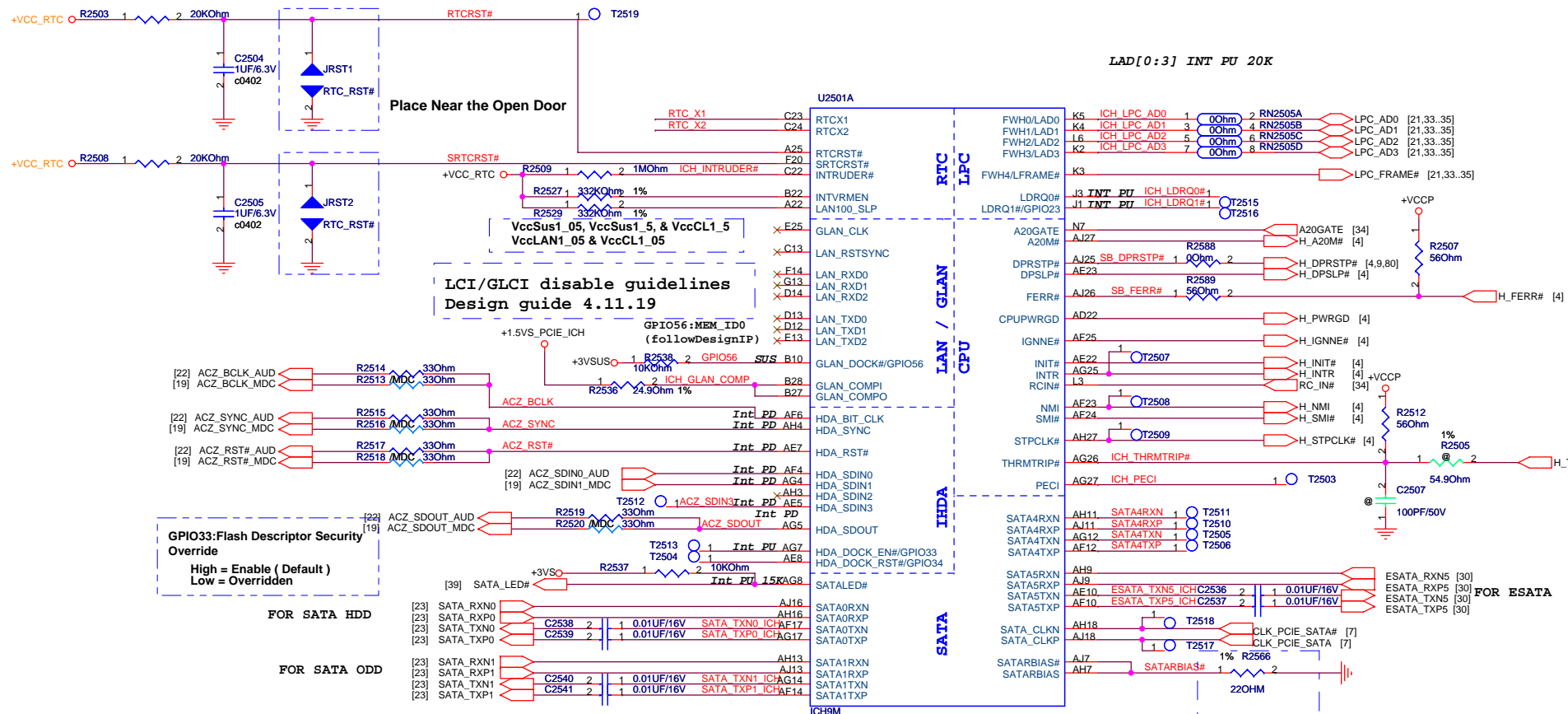
P/N: 12G151000138



<Variant Name>



<Variant Name>



[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

01= Enter XOR Chain

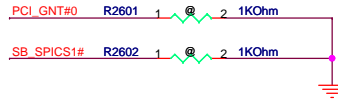
10= Normal Operation (Default)

11= Set PCIe Port Config Bit 1

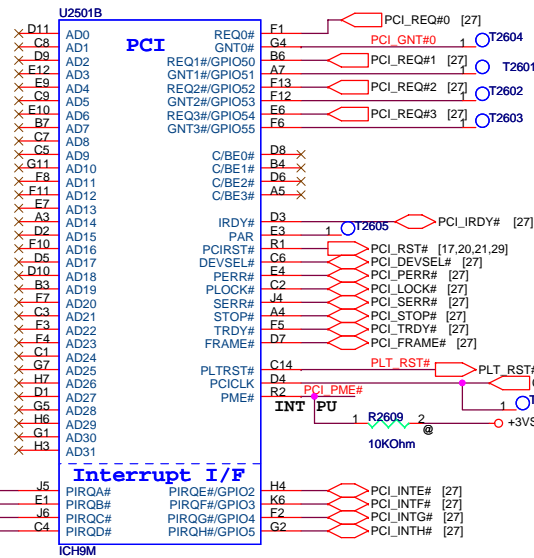


ICH9 Boot BIOS select

		GNT#0	SPICS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

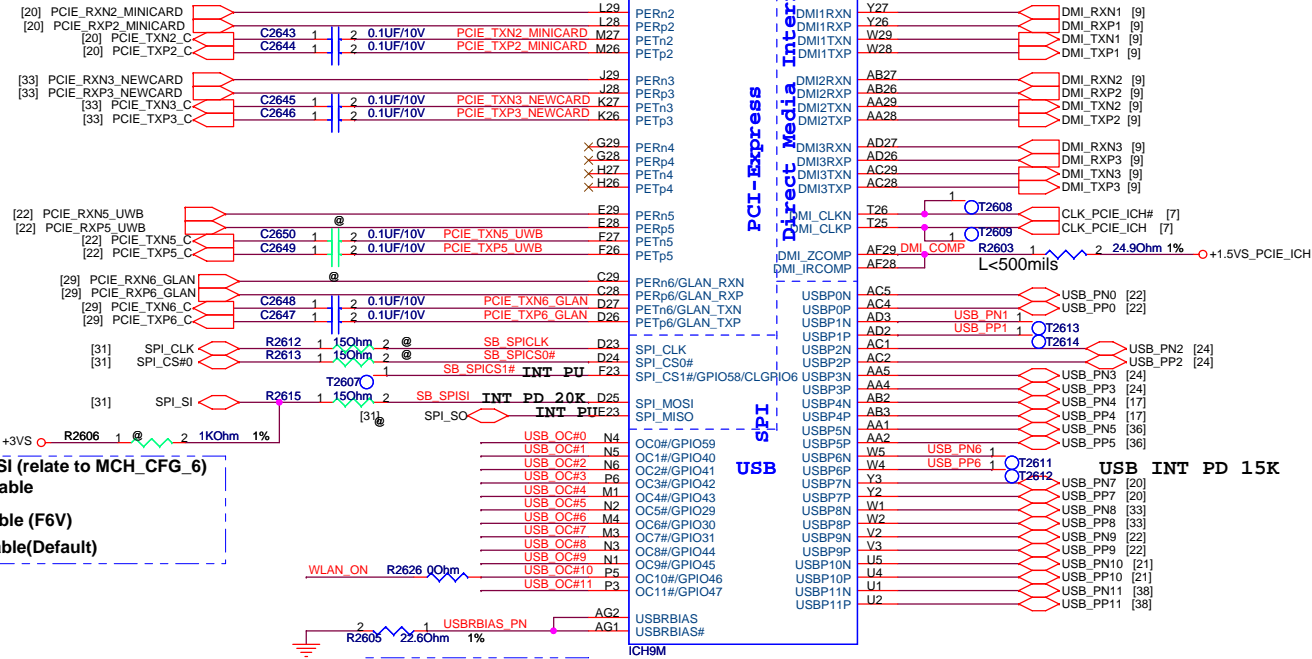


GNT#[0:3]:INT PU



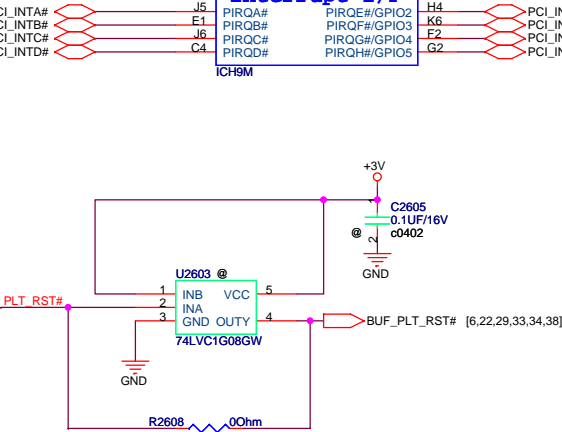
**SPI_MOSI (relate to MCH_CFG_6)
iTPM Enable**
H: Enable (F6V)
L: Disable(Default)

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	UWB
PCIE 6	LAN

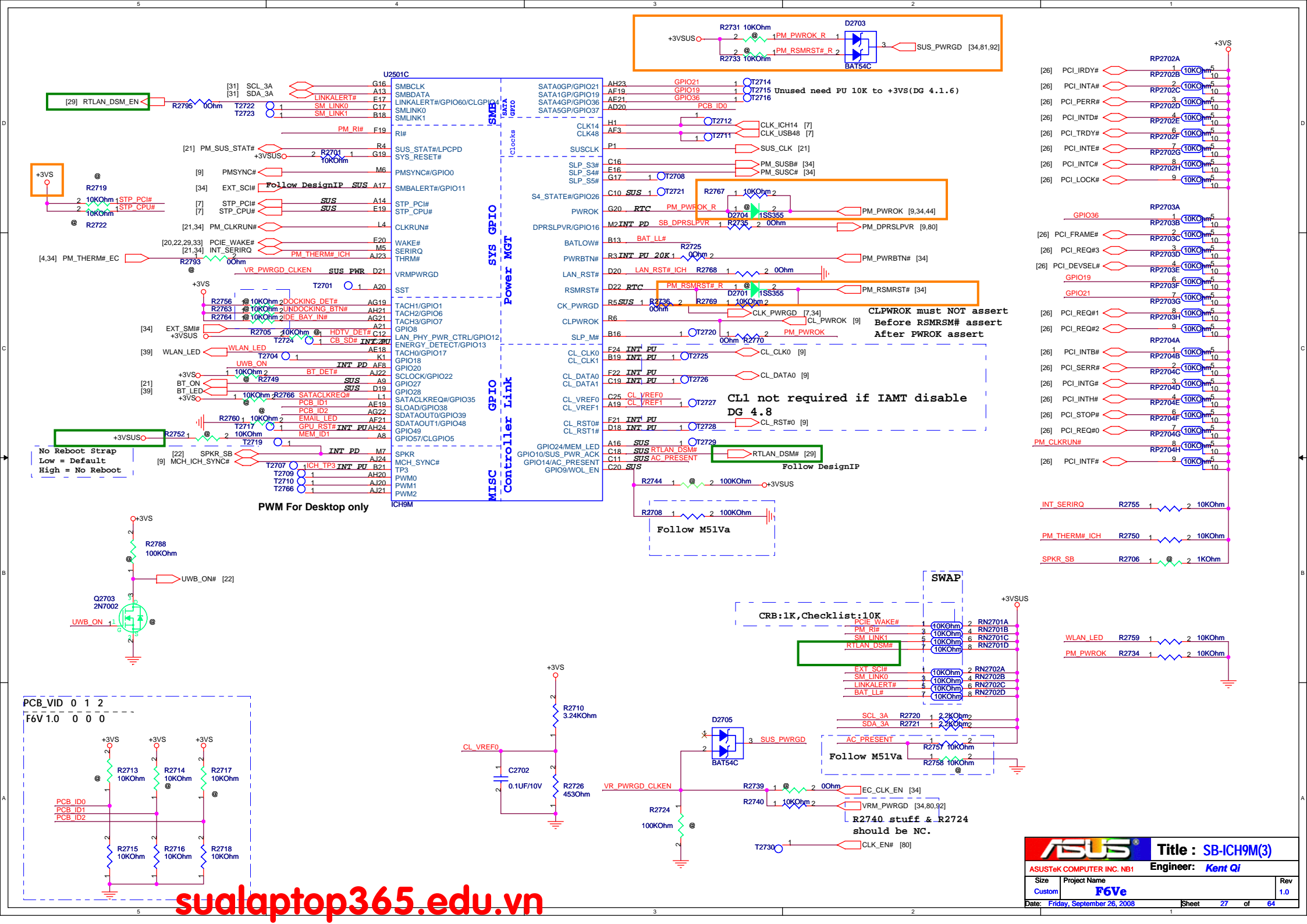


WLAN_ON R2626 0Ohm

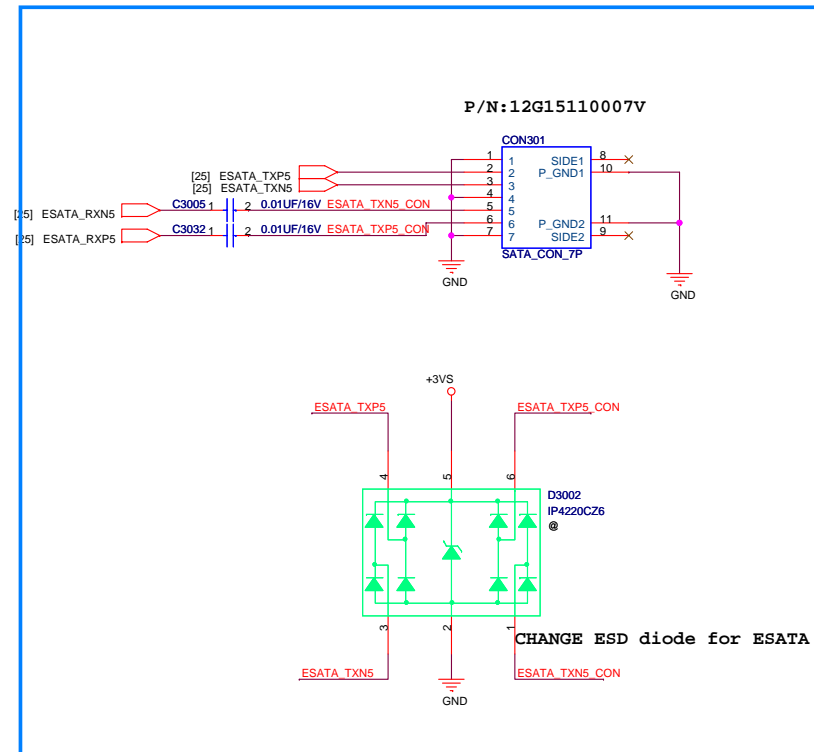
Place within 500 mils of ICH

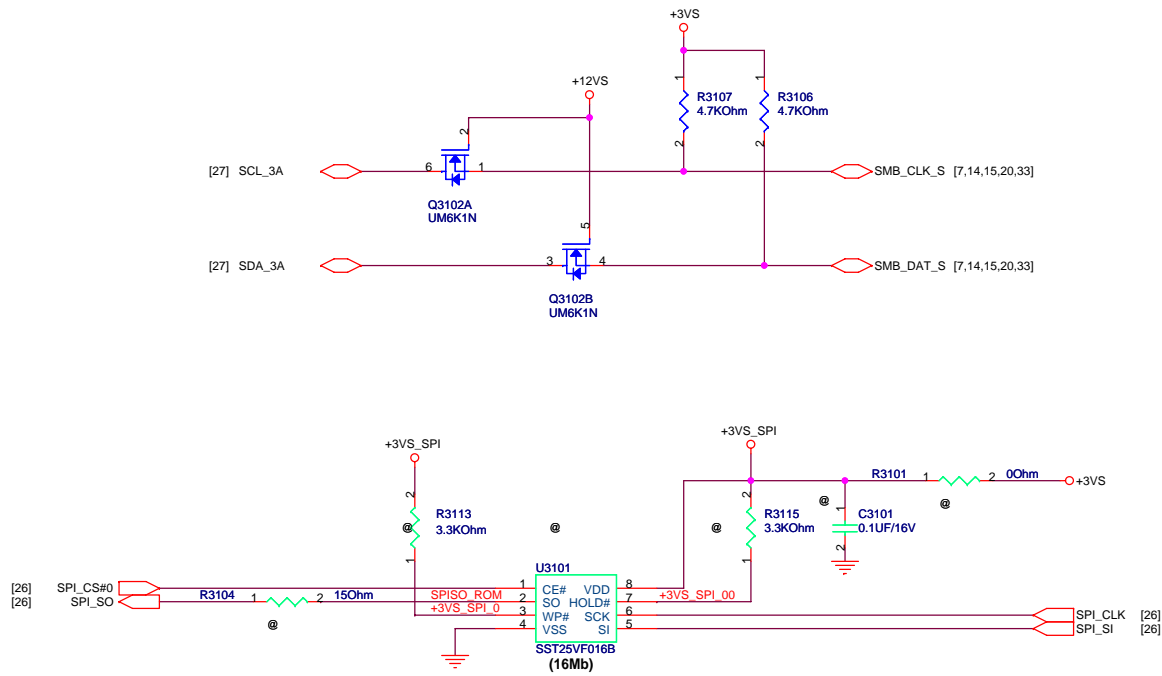


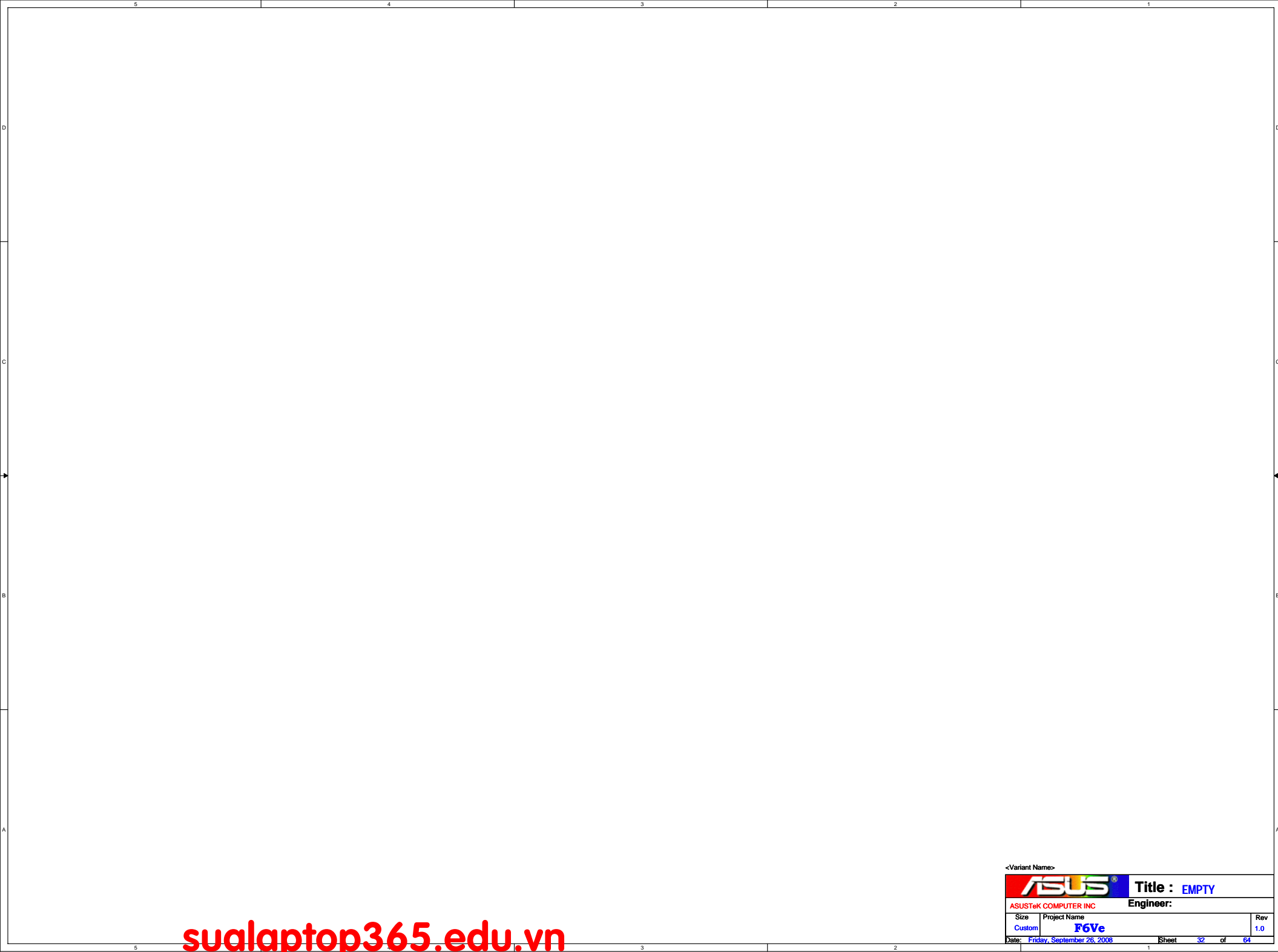
USB 0	USB Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	CMOS Camera
USB 5	CardReader
USB 6	UWB
USB 7	WiMax
USB 8	NewCard
USB 9	3G Card
USB 10	Bluetooth
USB 11	FINGER PRINT




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<Variant Name>



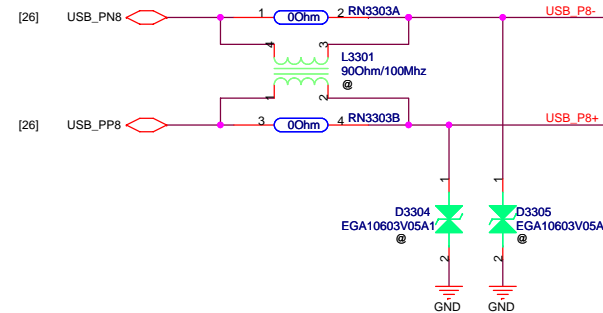
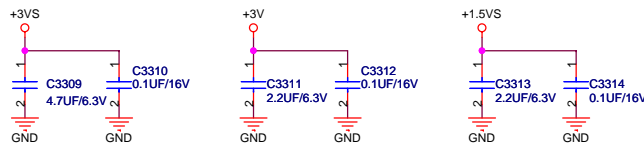
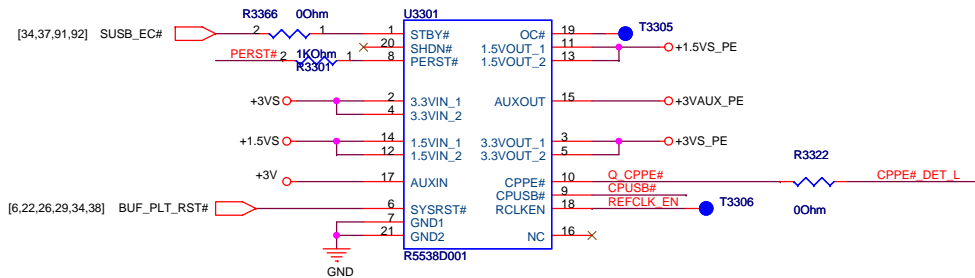
Title : EMPTY

ASUSTeK COMPUTER INC

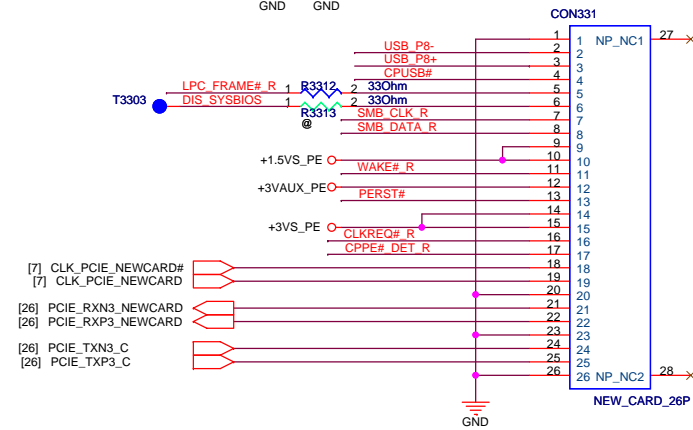
Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

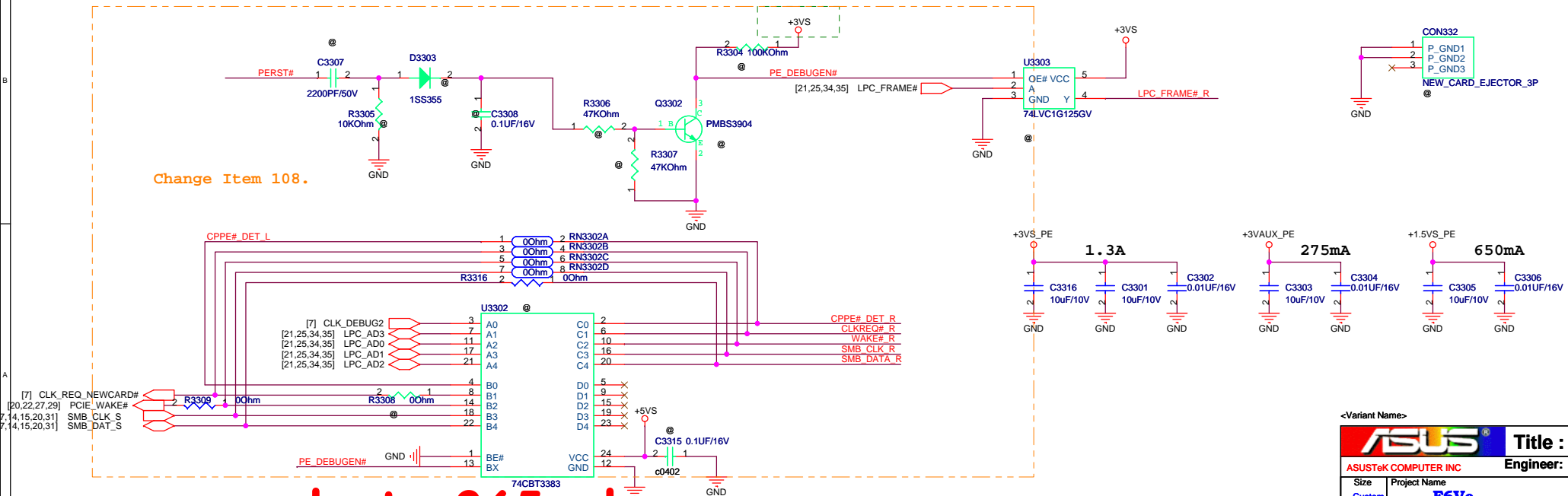
Date: Friday, September 26, 2008Sheet 32 of 64



NewCard Header
P/N:12G16130026R

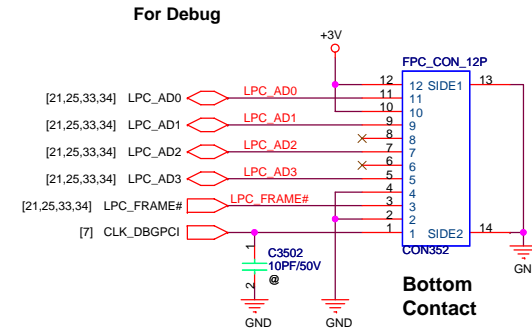


Change Item 108.



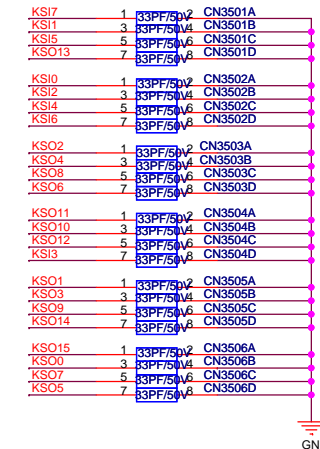
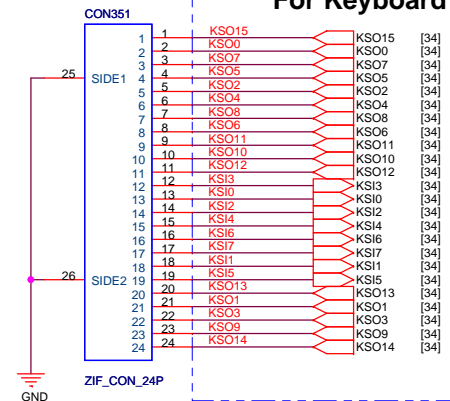
<Variant Name>

ASUS		Title : NEW CARD	
ASUSTeK COMPUTER INC		Engineer: Kent Qi	
Size	Project Name	Rev	
Custom	F6ve	1.0	
Date: Friday, September 26, 2008	Sheet	33	of 64

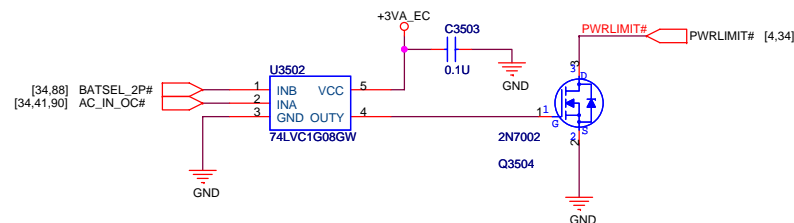


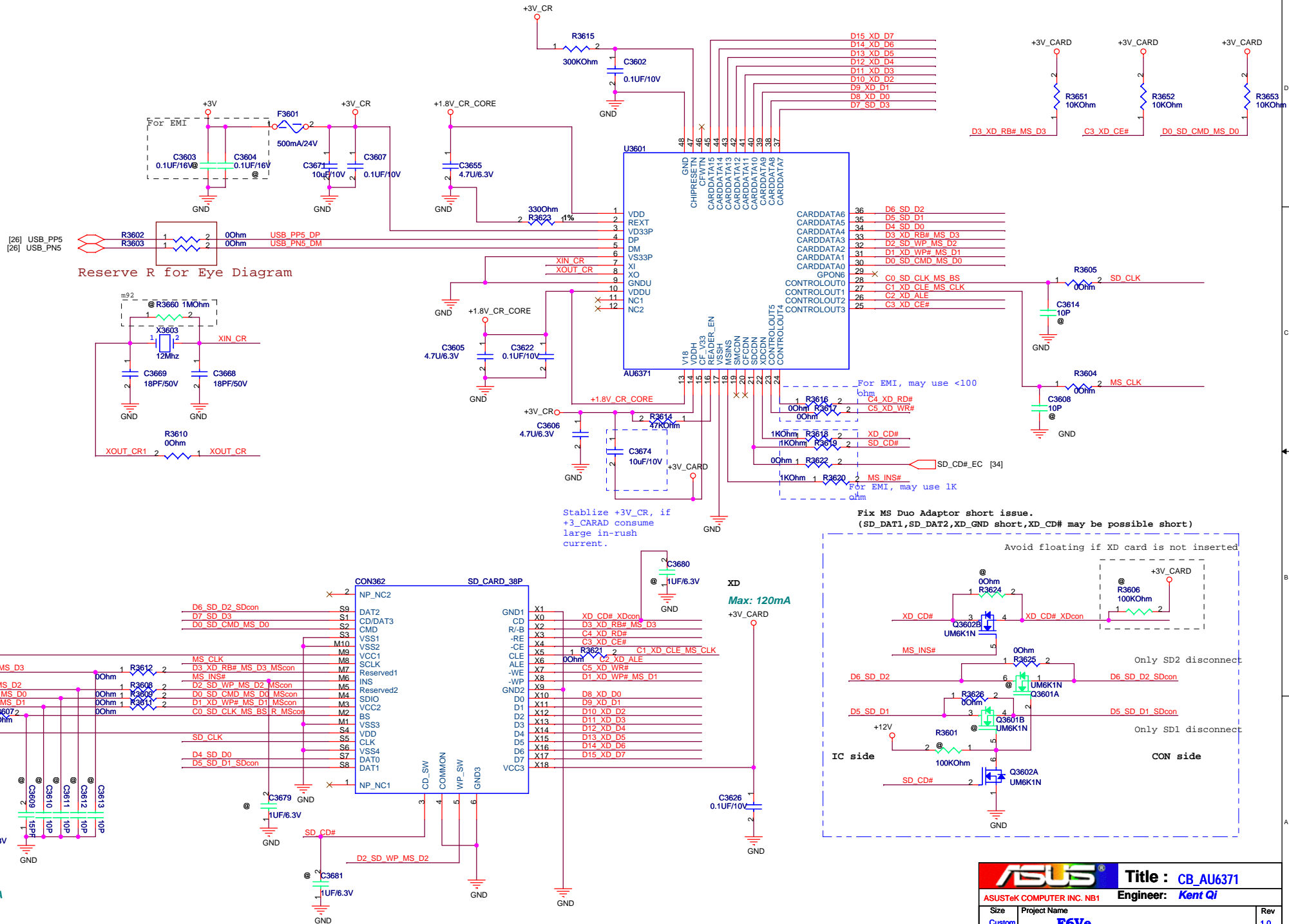
P/N:12G182402404

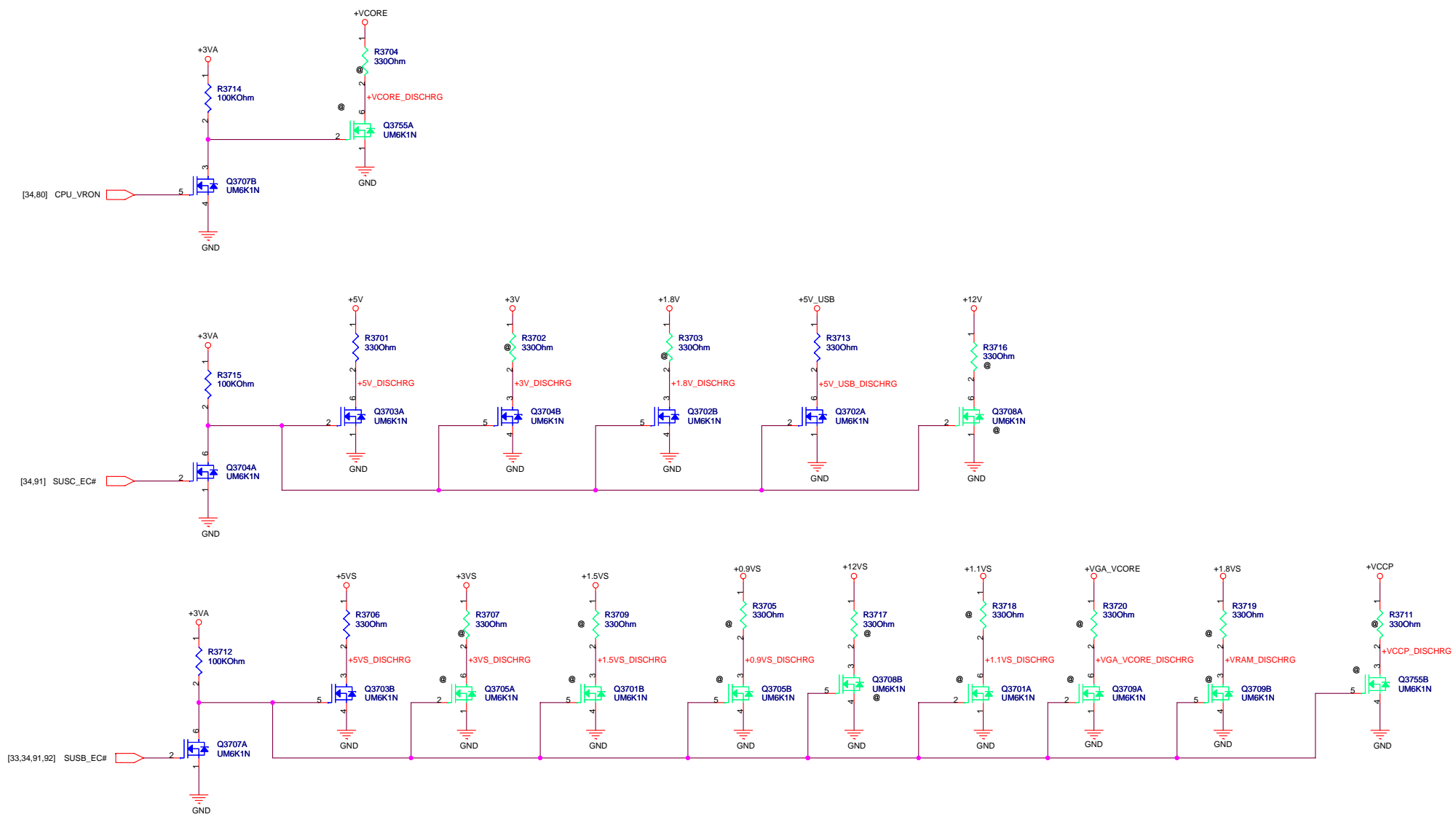
For Keyboard



PWRLMT Circuit: For Battery 1P



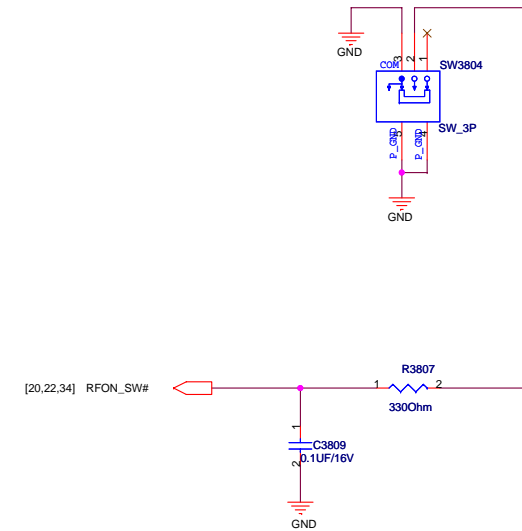
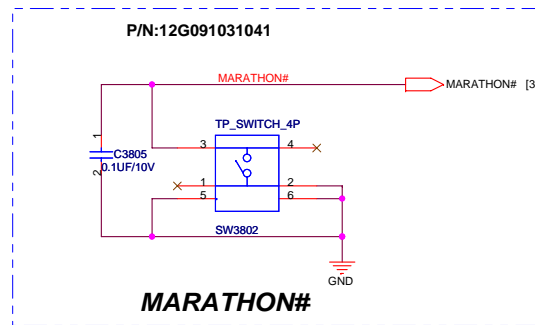




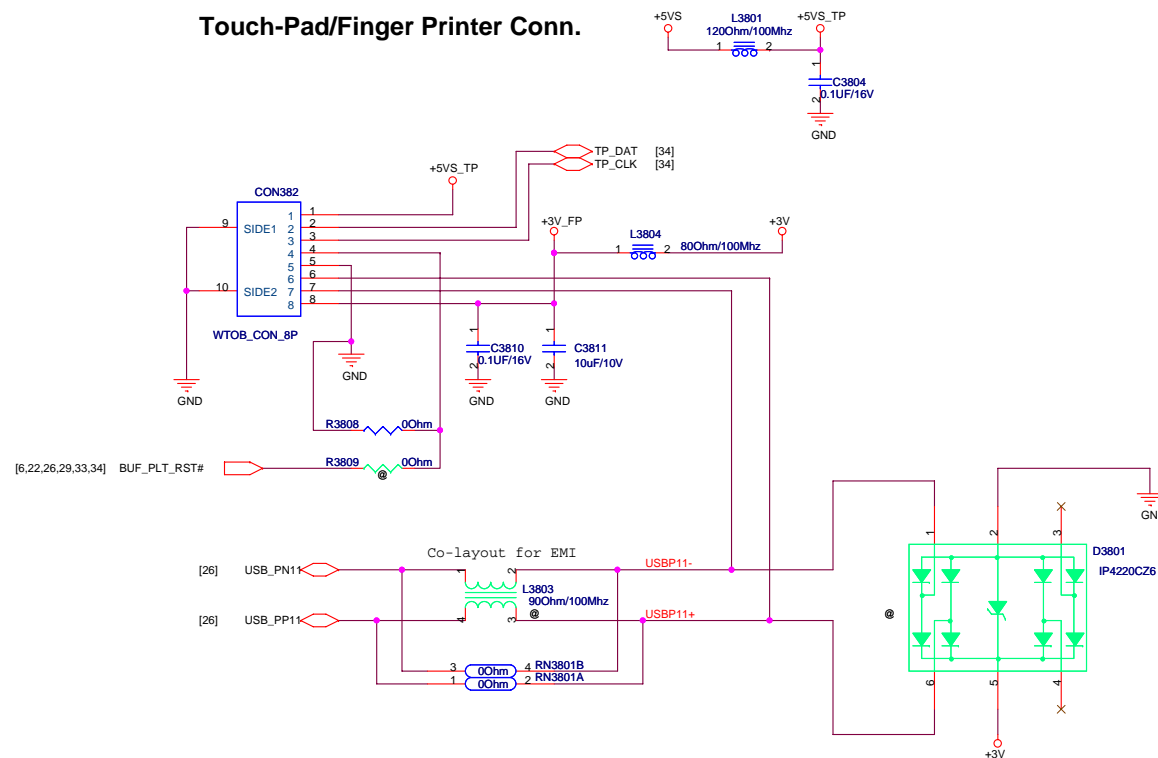
<Variant Name>

ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: Kent Qi	
Size	Project Name	Rev	
Custom	F6Ve	1.0	
Date: Friday, September 26, 2008		Sheet	37 of 64

BT/WLAN SW



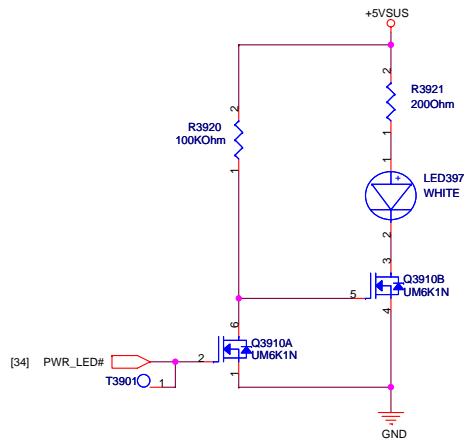
Touch-Pad/Finger Printer Conn.



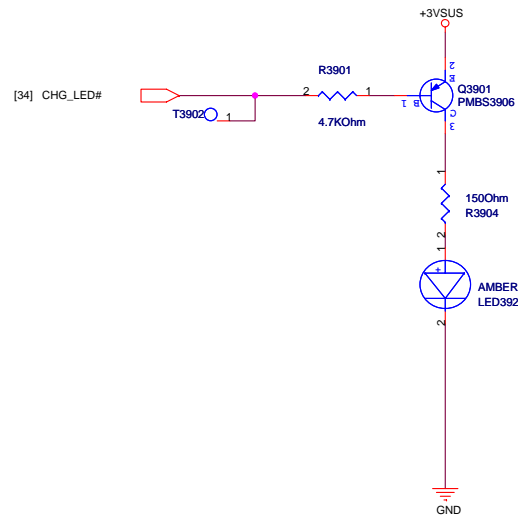
<Variant Name>

ASUS		Title : KEY & LED	
ASUSTeK COMPUTER INC		Engineer: Kent Qi	
Size	Project Name	Rev	
Custom	F6Ve	1.0	
Date: Friday, September 26, 2008		Sheet	38 of 64

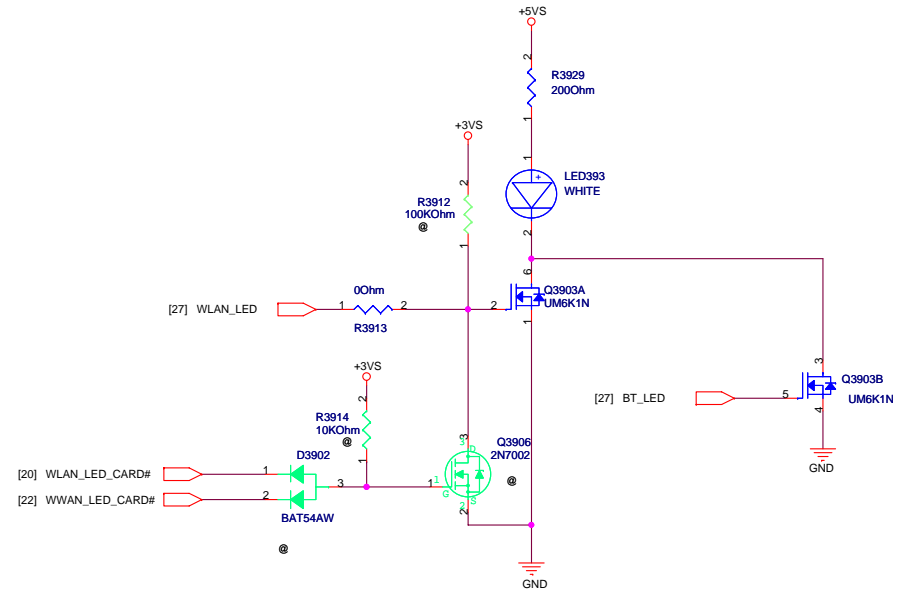
PWR LED



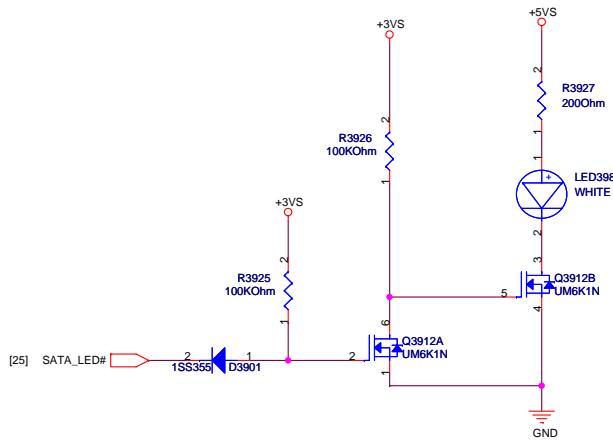
BATTERY LED



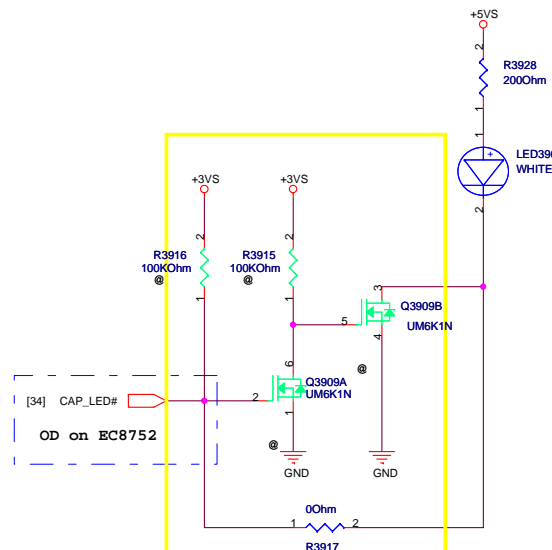
WireLess/BT LED

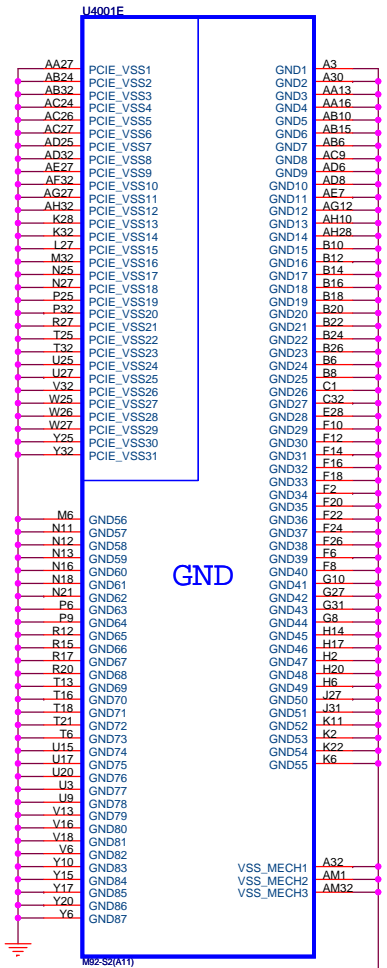


SATA LED



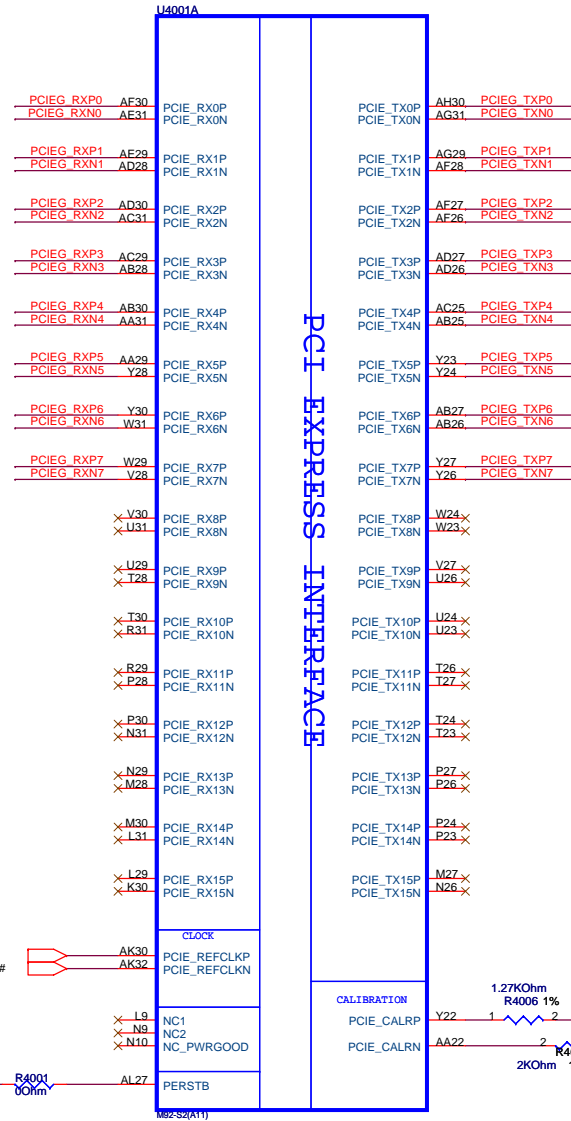
Cap. Lock





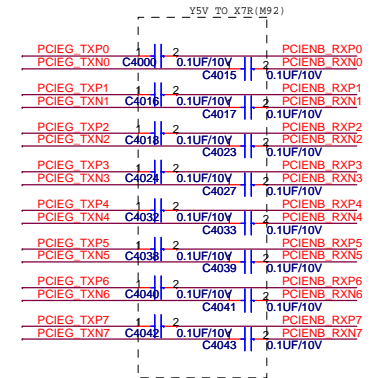
[9] PCIEG_RXP[0..7]

[9] PCIEG_RXN[0..7]



PCIEB_RXN[0..7] [9]

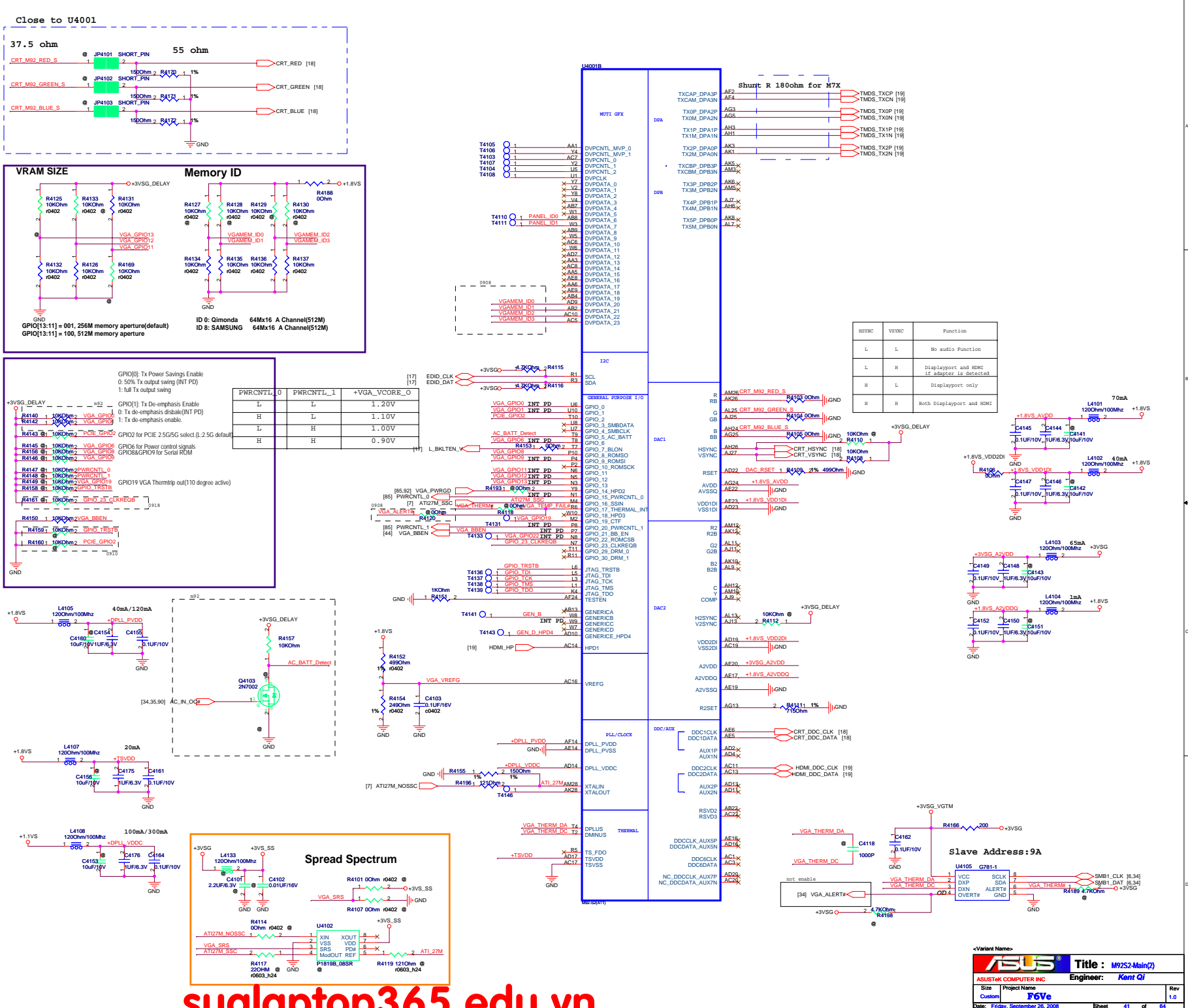
PCIEB_RXP[0..7] [9]

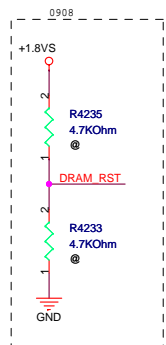
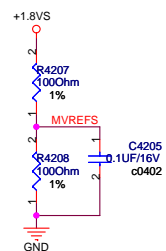
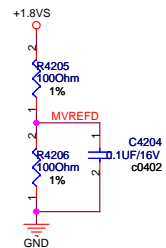


PCI EXPRESS INTERFACE

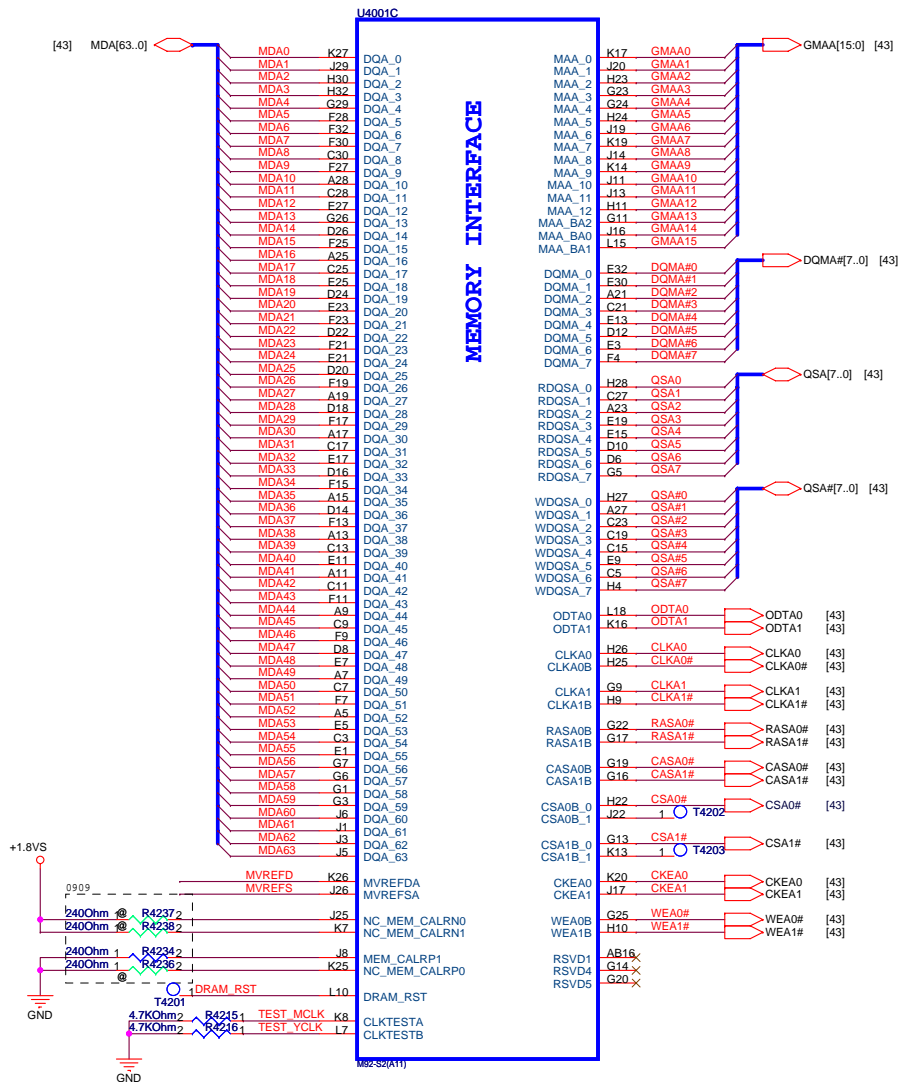
<Variant Name>

		Title : M92S2-PCIE(1)	
ASUSTeK COMPUTER INC		Engineer: Kent Qi	
Size	Project Name	Rev	
Custom	F6Ve	1.0	
Date: Friday, September 26, 2008		Sheet 40 of 64	





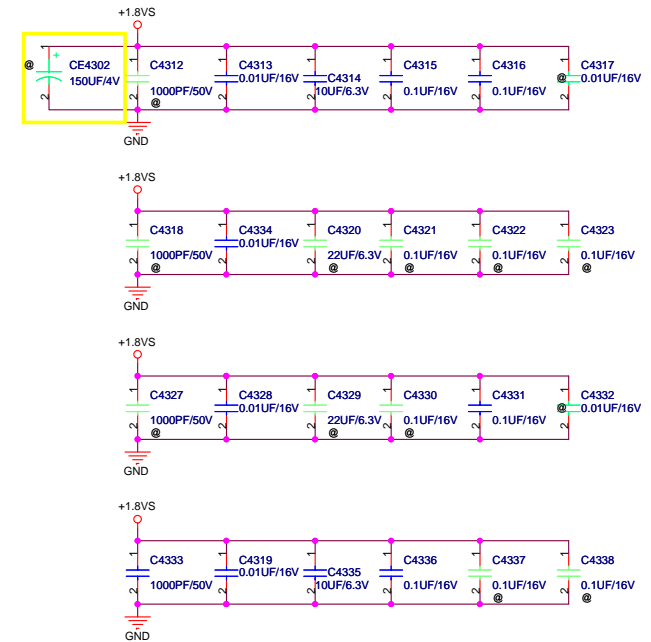
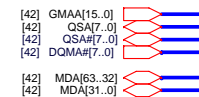
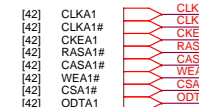
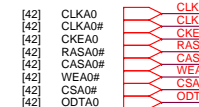
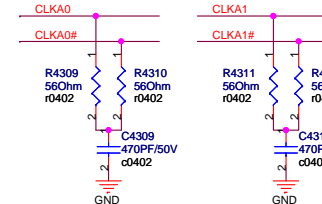
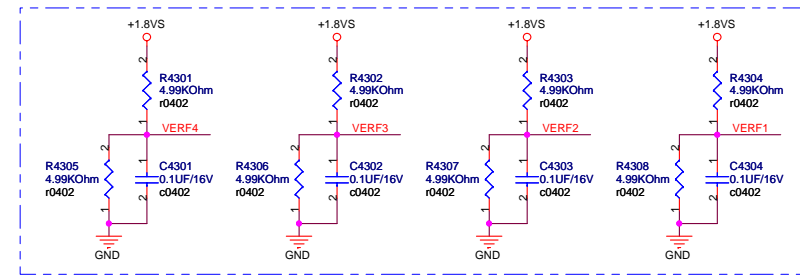
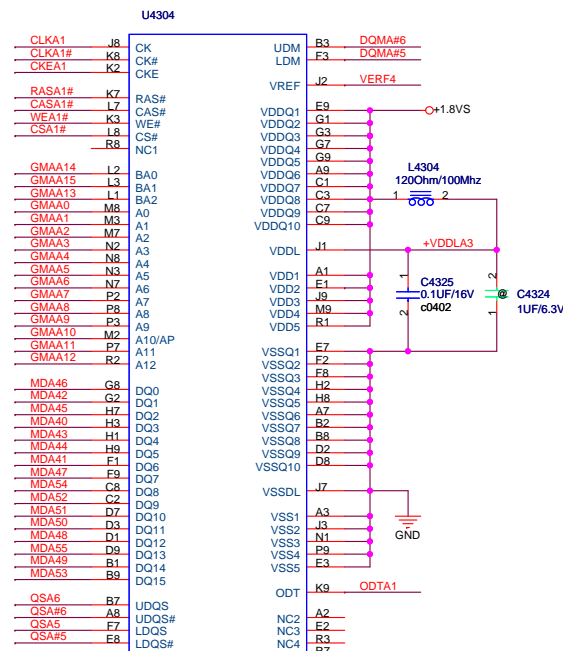
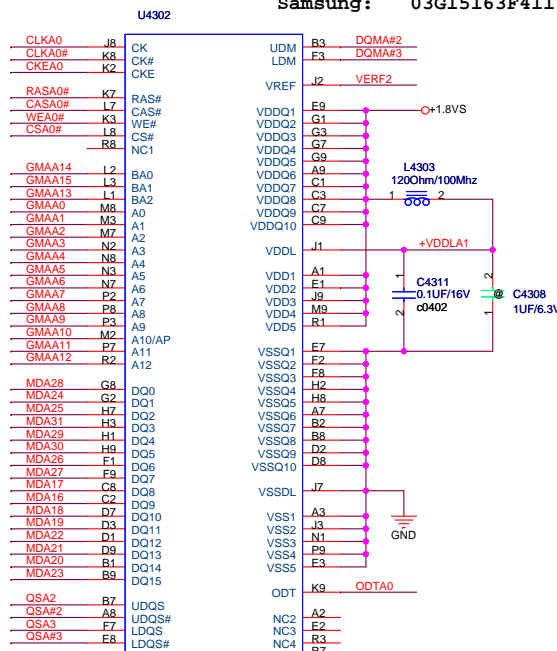
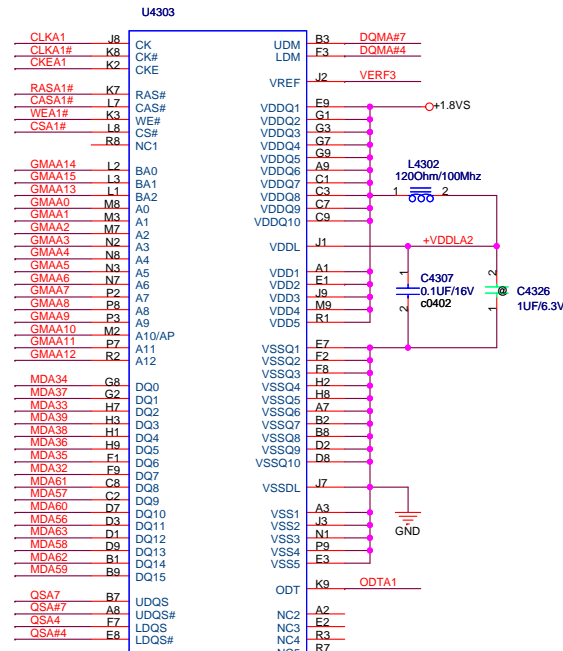
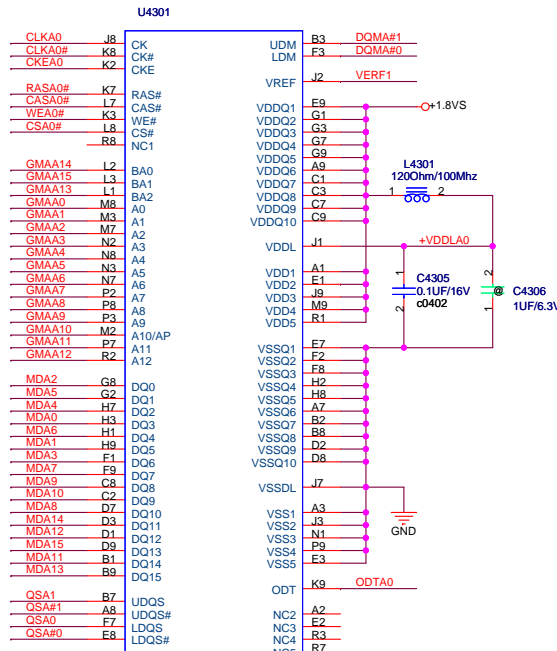
DRAM_RST NC for DDR2



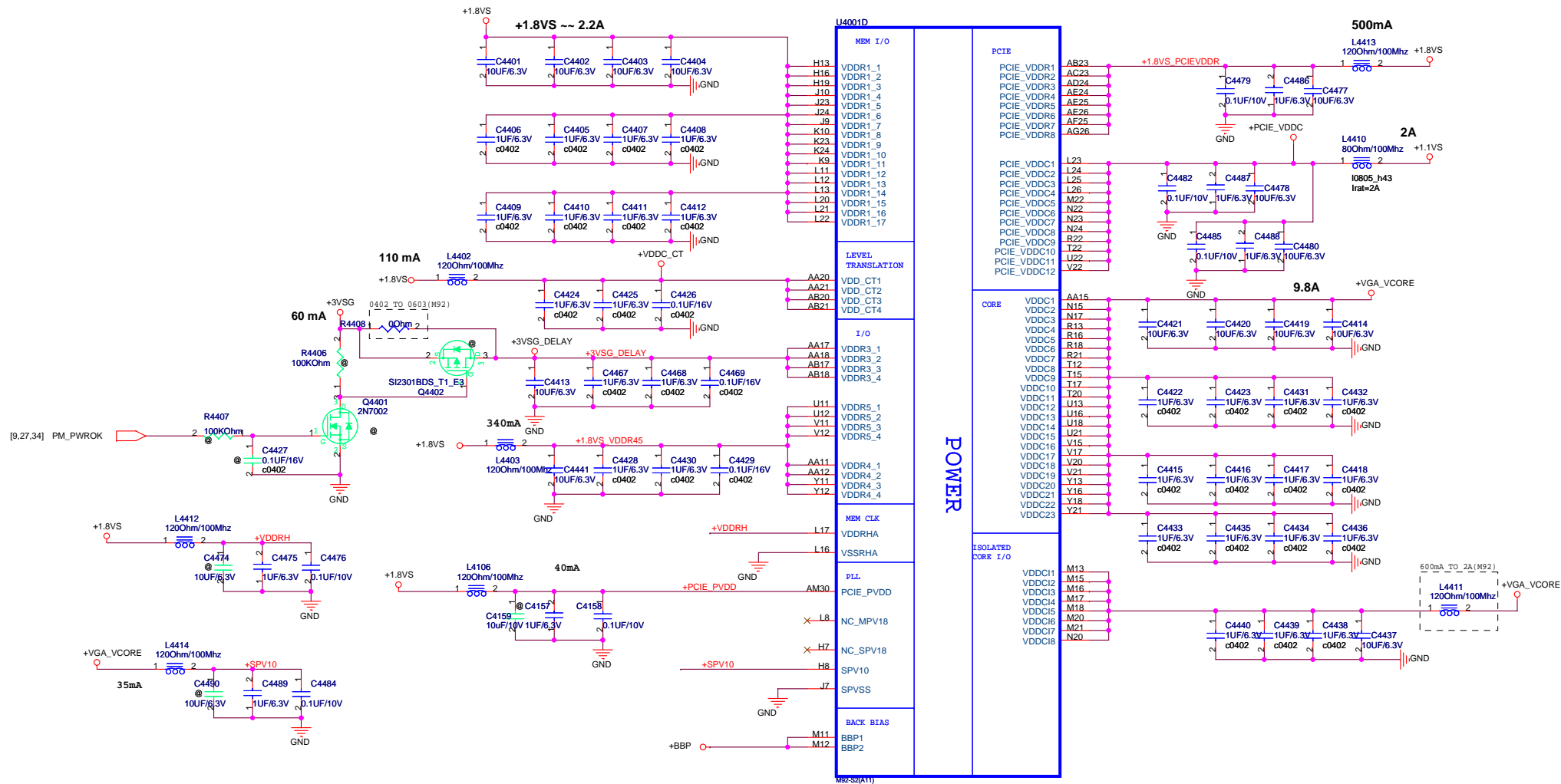
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

<Variant Name>

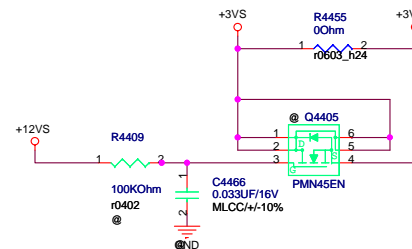
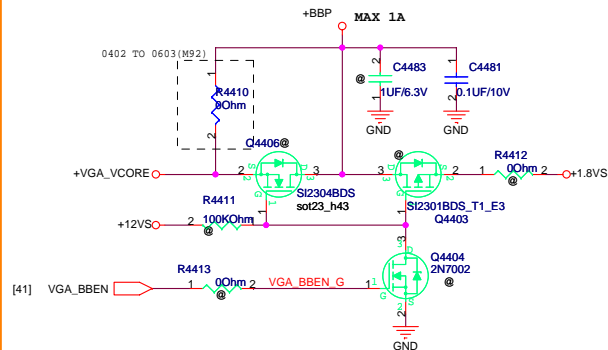
ASUS		Title : M92S2-MEM CTRL(3)	
ASUSTeK COMPUTER INC		Engineer: Kent Qi	
Size	Project Name	Rev	
Custom	F6Ve	1.0	
Date: Friday, September 26, 2008		Sheet	42 of 64



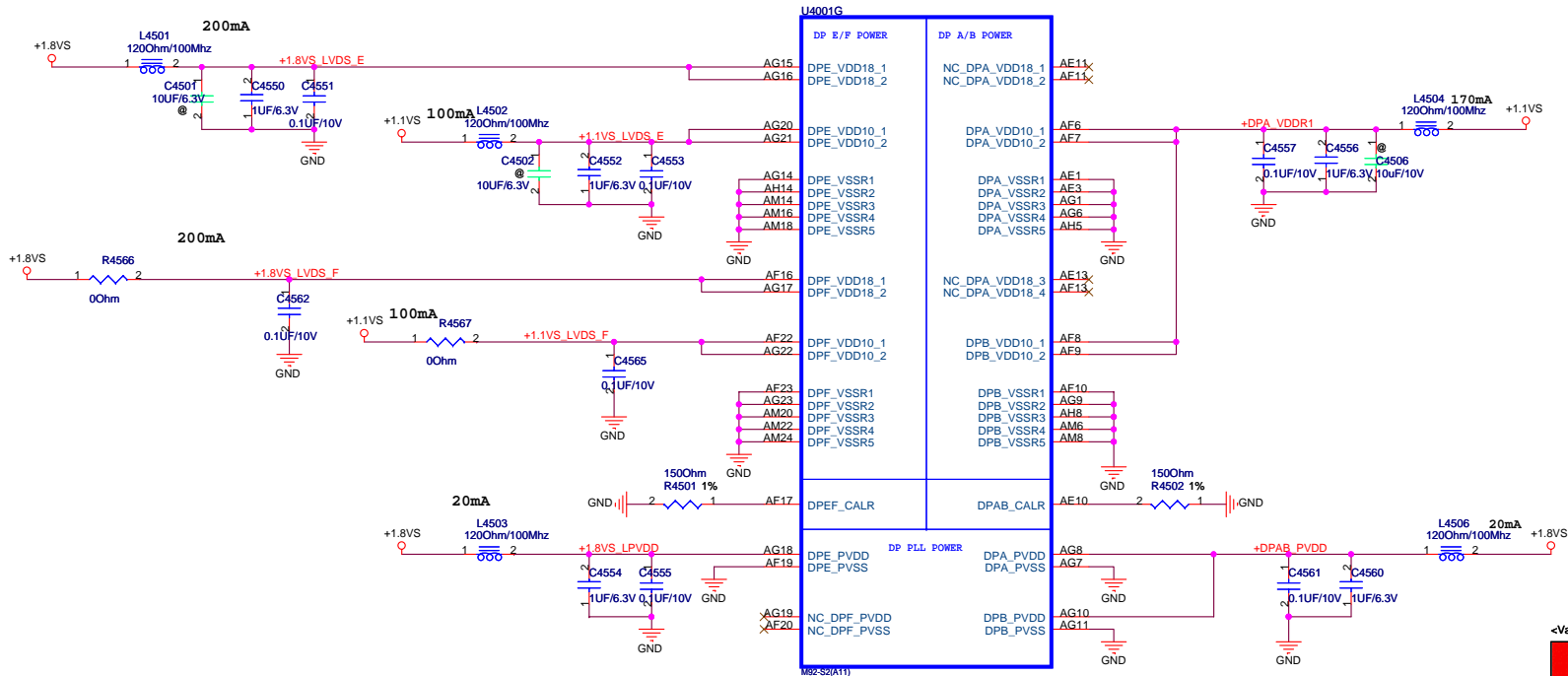
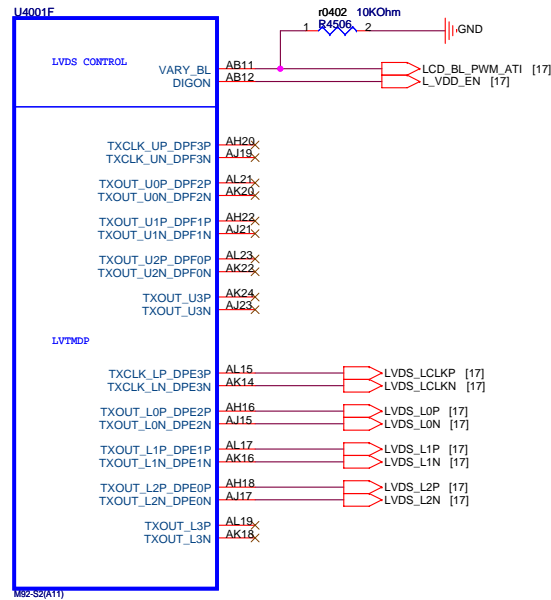
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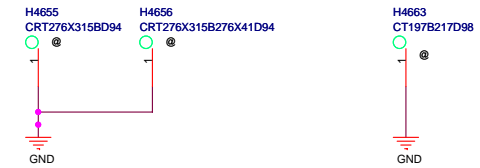
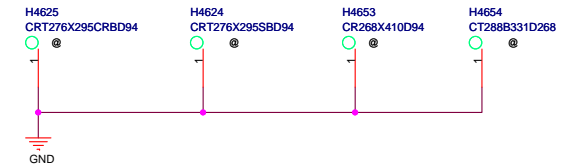
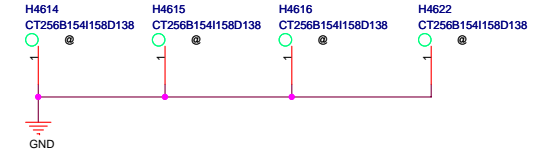
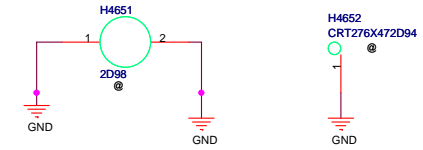
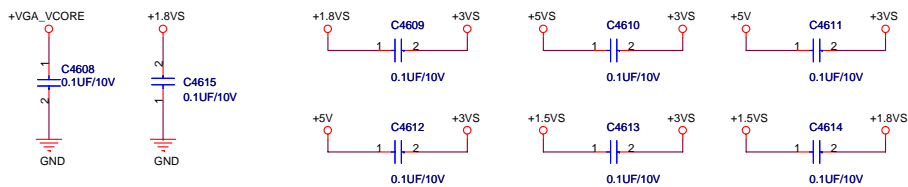
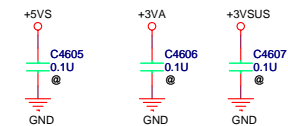
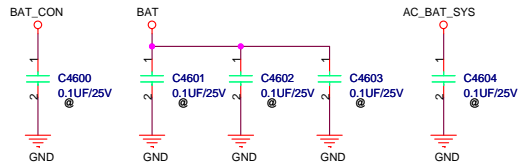
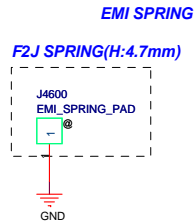
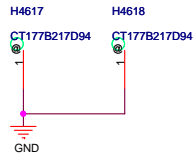


BBN could tie to GND directly for ATI suggestion.
Thus, MAX1673ESA could be save.

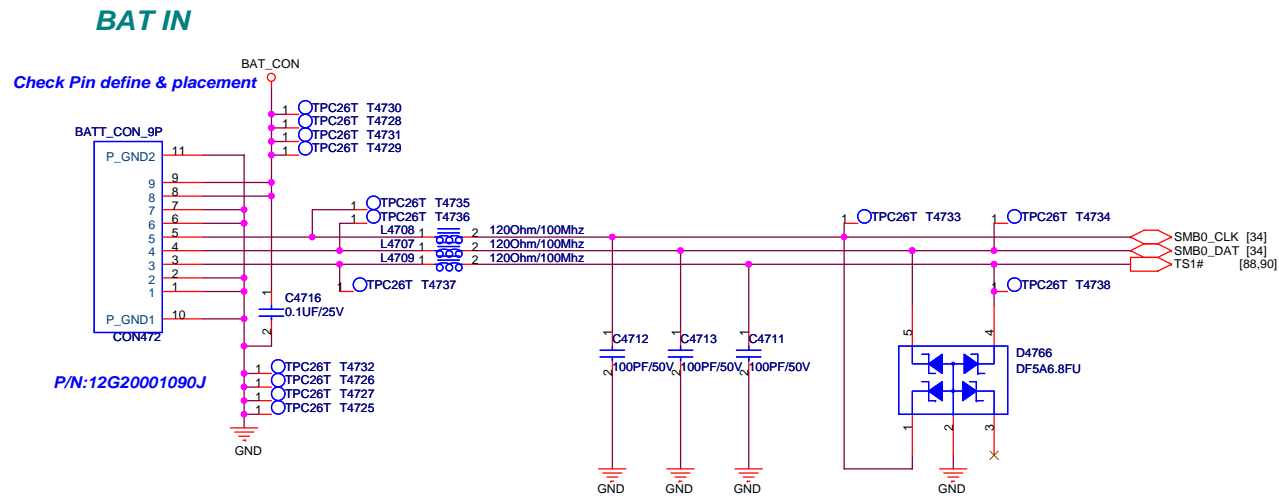
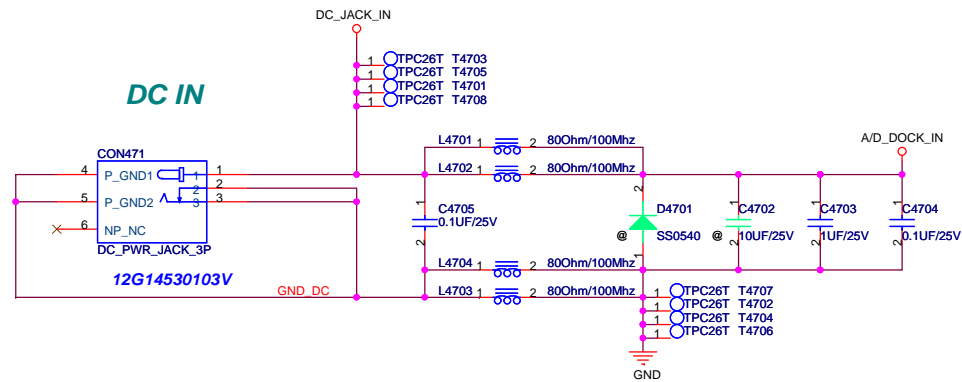


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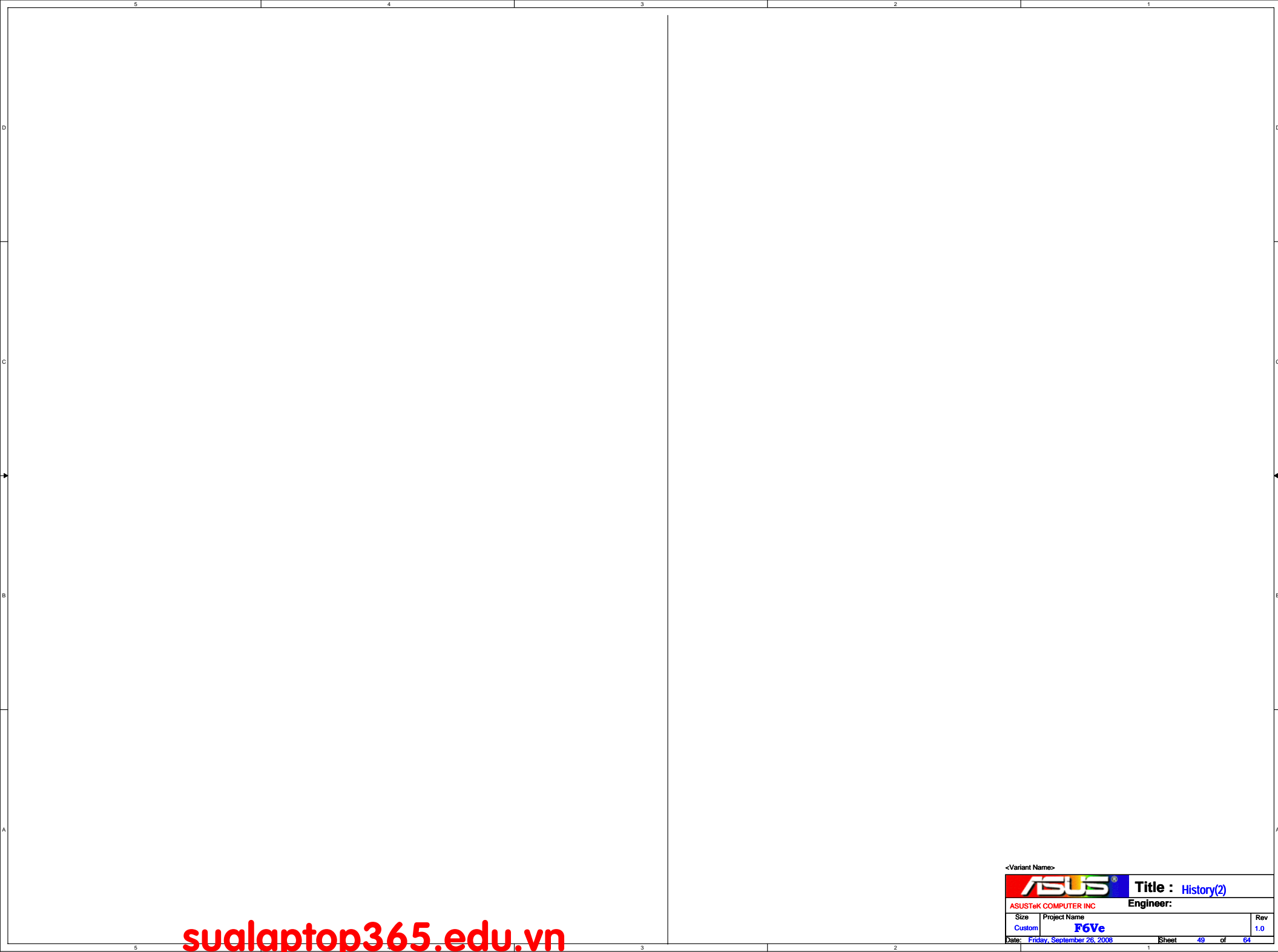


<Variant Name>		Title : SCREW HOLE	
ASUS®		Engineer:	
Size	Project Name	Rev	
Custom	F6Ve	1.0	
Date: Friday, September 26, 2008	Sheet	46	of 64

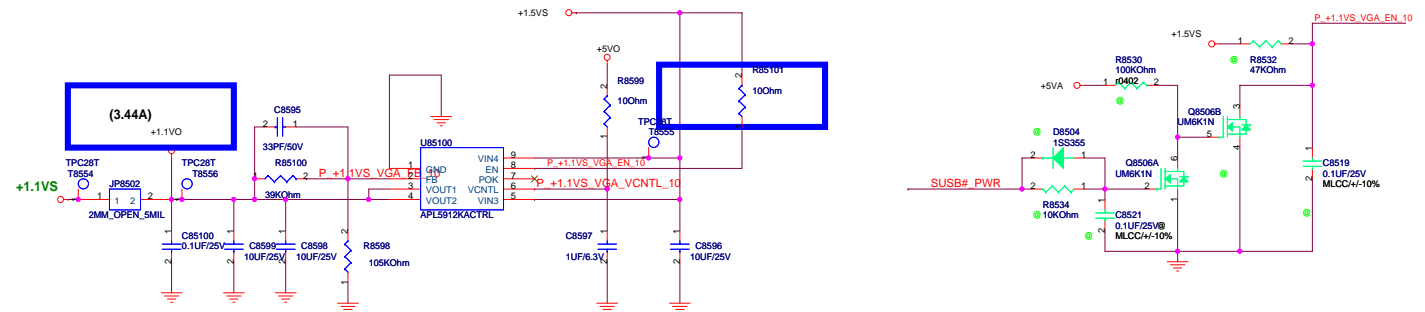


F6V-->F6Ve modify

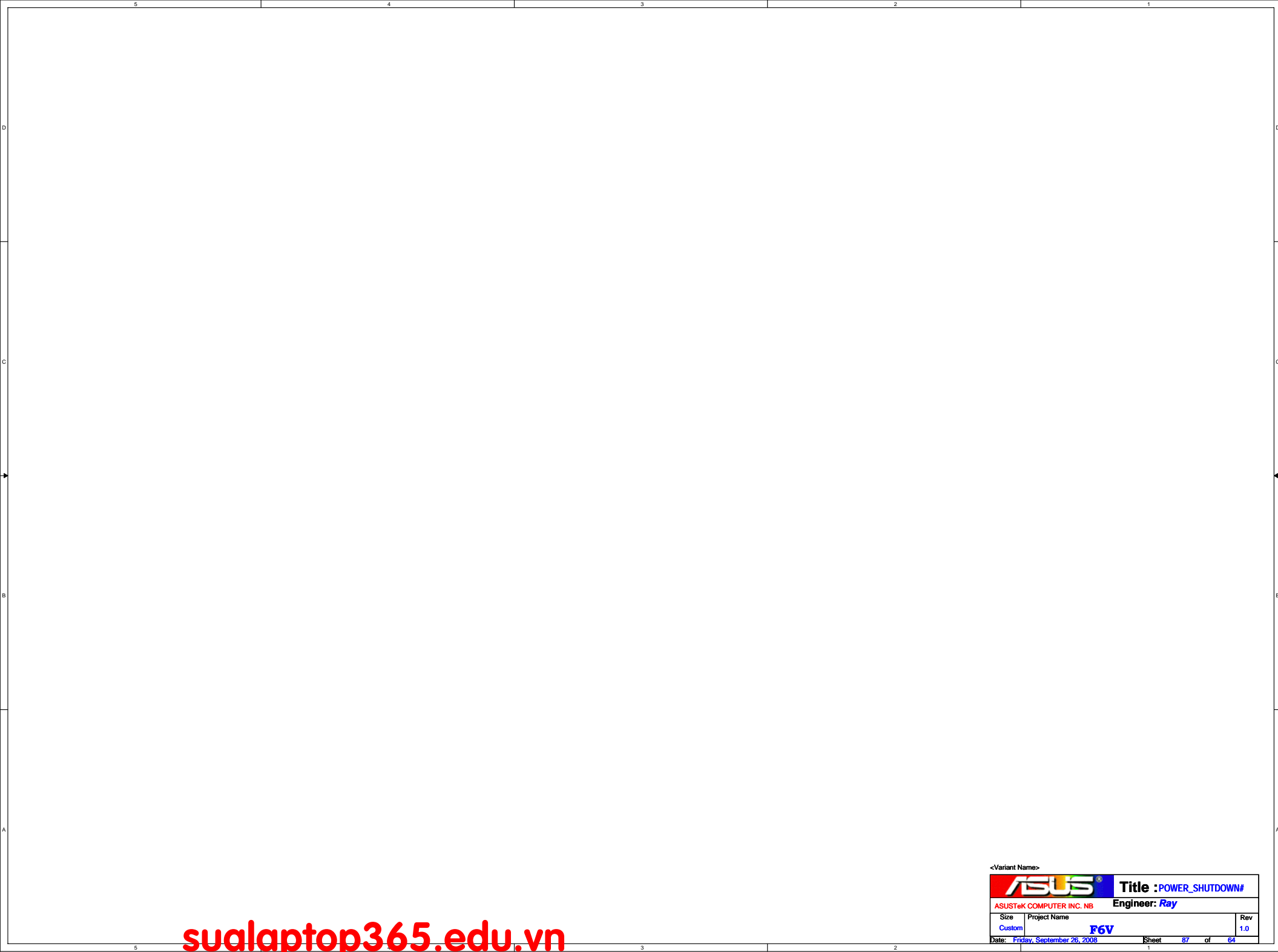
- 9.1.1,Page40~45:Change GPU M82_SE to M92-S2
- 9.1.2,Page40:change PCIE series capacitance from Y5V to X7Y
- 9.1.3,Page44:change R4408 R4410 from 0402 to 0603 and change L4411 from 600mA to 2A for current
- 9.1.4,Page22:change R2002 from 0603 to 0805 for current
- 9.1.5,Page22:remove R2201 for current
- 9.2.1,Page36:reserved R3660 for crystal X3603
- 9.2.2,Page34:place R3439 for MARATHON# pull up +3VA_EC
- 9.2.3,Page17:remove F1702(INVERTER Pin19) for cost down
- 9.2.4,Page12:add R1210 and C1243 for VCCD_QDAC to 1.5VS
- 9.2.5,Page33:add R3309 for PCIE_WAKE
- 9.4.1,Page43:change same net name to divided different name, +1.8Vs_LVDS-->+1.8Vs_LVDS_E and +1.8Vs_LVDS_F, +1.1Vs_LVDS-->+1.1Vs_LVDS_E and +1.1Vs_LVDS_F
- 9.4.2,Page41:change R4188 to 0603 for current
- 9.5.1,Page40:remove PCIE_[8..15] for layout
- 9.5.2,Page41:Place R4140 R4142 prevent can not link
- 9.5.3,Page41:reserved Q4103 R4157 for AC_BATT_Detect
- 9.8.1,Page41:move memory ID from DPVDATA[0..3] to DPVDATA[20..23]
- 9.8.2,Page41:reserved R4235 for DRAM_RST pull up
- 9.8.3,Page41:reserved R4120,connect GPIO_17_thermal to EC for thermal protect.
- 9.9.1,Page29:change L2904 L2903 to R2900 R2901
- 9.9.2,Page17:change R1717 from 100K to 10K,change R1718 from 1M to 10K
- 9.9.3,Page42:reserved R4237 R4238 for pull up NC_MEM_CALRN0 and NC_MEM_CALRN1 to +1.8VS, reserved R4236 for pull down NC_MEM_CALRP0 to ground
- 9.9.4,Page17:reserved R4159 R4160 for GPIO_TRSTB and PCIE_GPIO2 pull down
- 9.18.1,Page41:reserved R4161 for GPIO_23_CLKREQB pull up.







<Variant Name>		Title : <i>N/A</i>	
		ASUSTeK COMPUTER INC. NB Engineer: <i>Ray</i>	
Size B	Project Name F6V	Rev 1.0	
Date: Friday, September 26, 2008		Sheet	86 of 64



POWER PATH & BAT_LEARN

90 WATT

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter lin(max) = $[0.075V/Rsense(ADin)] \cdot [VCLS/REF]$
 $Rsense(ADin) = 0.010ohm$
 $VCLS = 2.5341V$
 $\Rightarrow lin(max) = 4.5A$
 $\Rightarrow Constant Power = 19 \cdot 4.5 = 85.5W$
 $\Rightarrow R5710 = 20K, R5715 = 30K$

Charge Current $I_{chg} = [0.075V/Rsense(CHG)] \cdot [VICTL/3.6V]$
 $Rsense(CHG) = 0.025ohm$
 $VICTL = 3V \Rightarrow I_{chg} = 2.5A$
 $VICTL = 1.68V \Rightarrow I_{chg} = 1.4A$

$V_{batt} = Cell \cdot \{ V_{ref} + (VICTL - 1.8V) / 9.52 \}$
 $VICTL = 1.588V \Rightarrow V_{batt} = 4.2V$

Mode pin : $V_{mode} > 2.6V$ (tie to LDO pin) \rightarrow 4 Cells
 $2.0 > V_{mode} > 1.6V$ (floating) \rightarrow 3 Cells
 $0.8 > V_{mode}$ (tie to GND) \rightarrow Learning mode

$VICTL < 0.8V$ or $DCIN < 7V \rightarrow$ Charger Disable

Preccharge current=150mA

[34,35] BATSEL_2P#

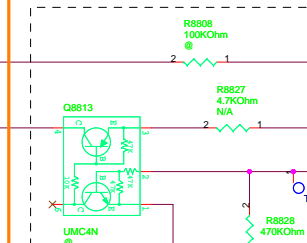
[34] PRECHG

[34] CHG_EN#

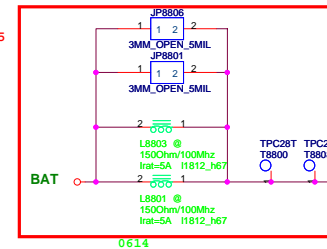
[34] BAT_LEARN

071015

4S: Mount R8808 only
 3S: Unmount all components
 3S/4S: Unmount R8808, and mount others

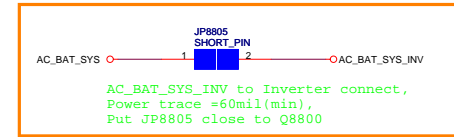


071015



0614

070115

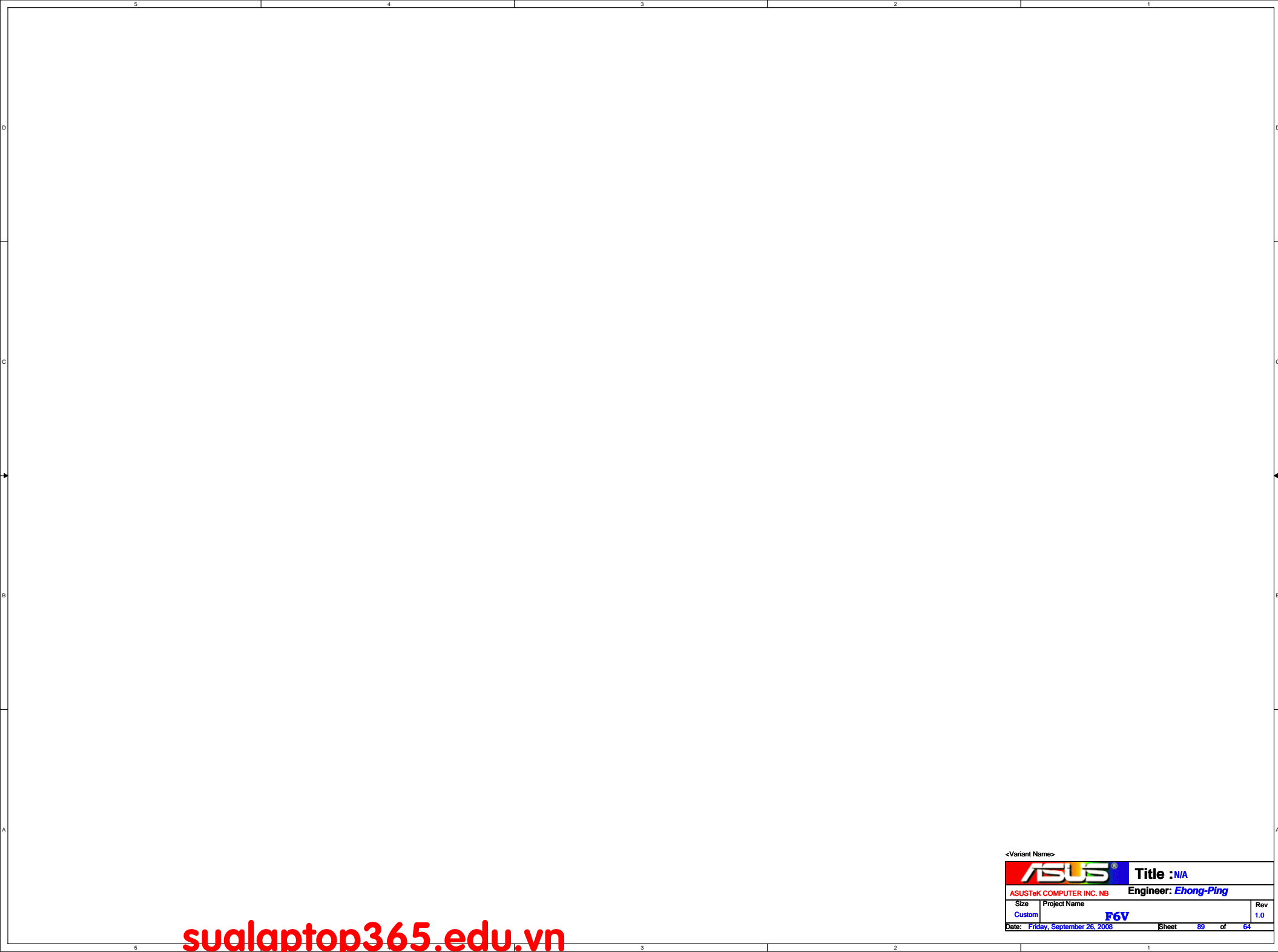


AC_BAT_SYS_INV to Inverter connect,
Power Trace = 60mil(min),
Put JP8805 close to Q8800

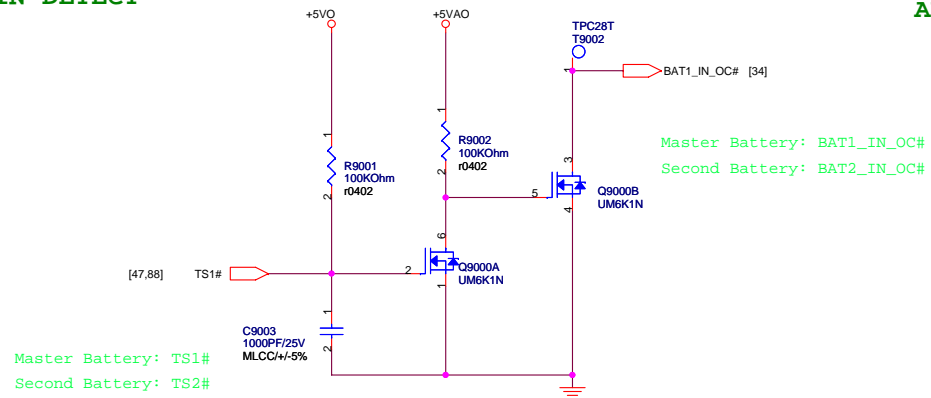
071015

<Variant Name>

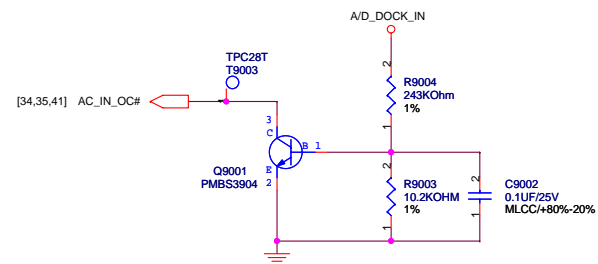
ASUS		Title : POWER_CHARGER	
ASUSTek COMPUTER INC. NB		Engineer:	
Size	Project Name		Rev
Custom			1.0
Date: Friday, September 26, 2008		Sheet 88 of 84	



BATTERY IN DETECT



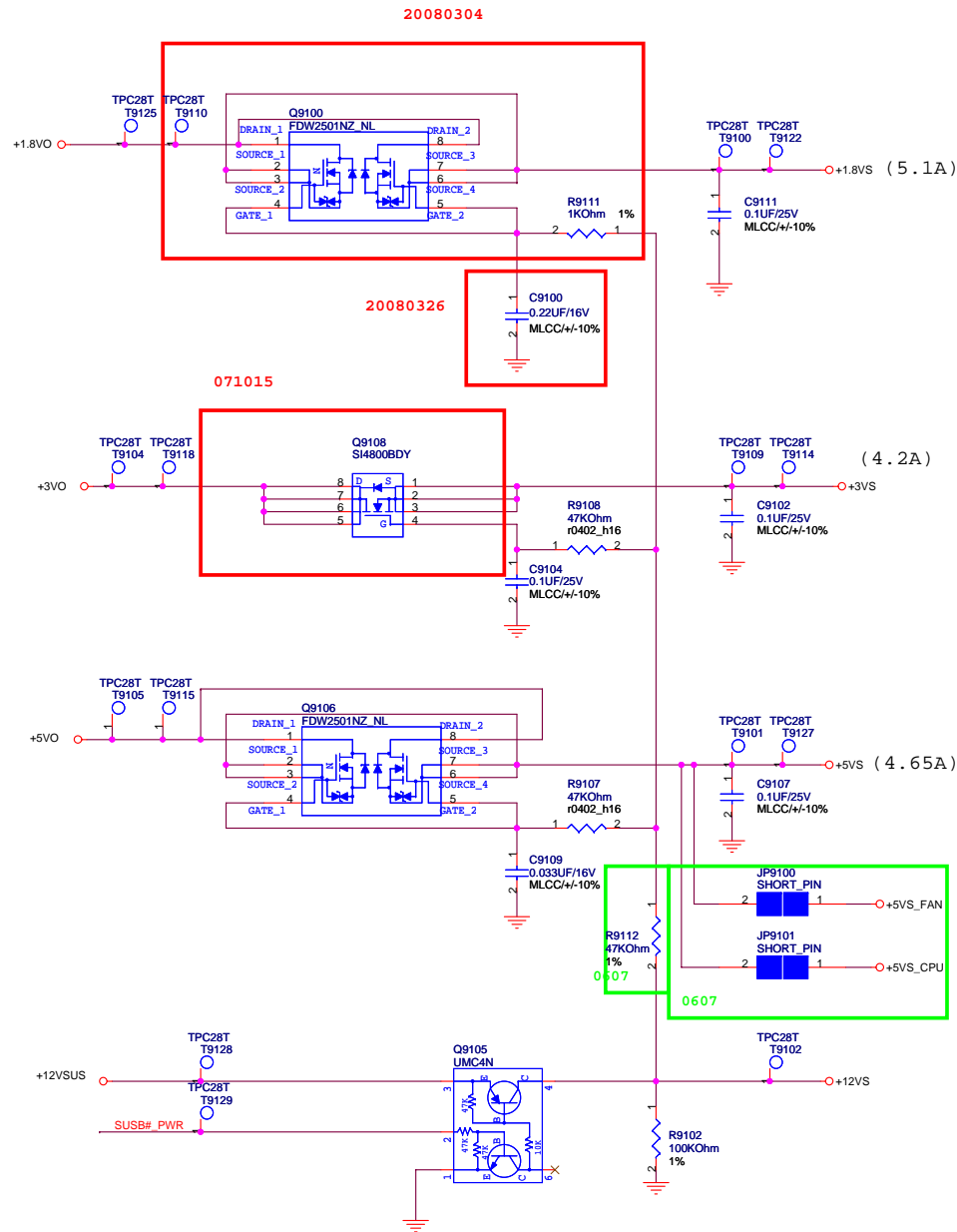
ADAPTER IN DETECT



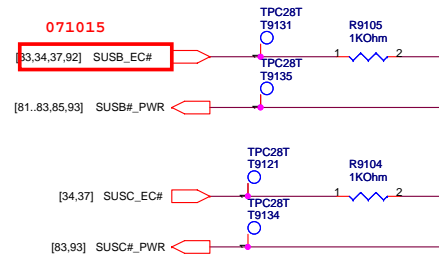
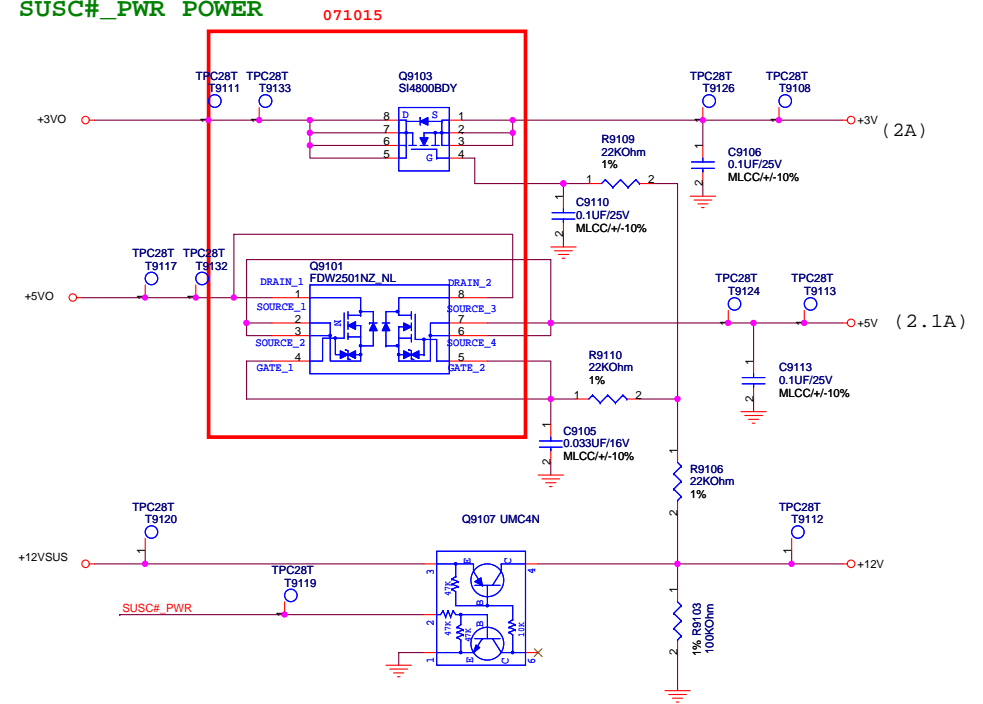
+2.5VREF

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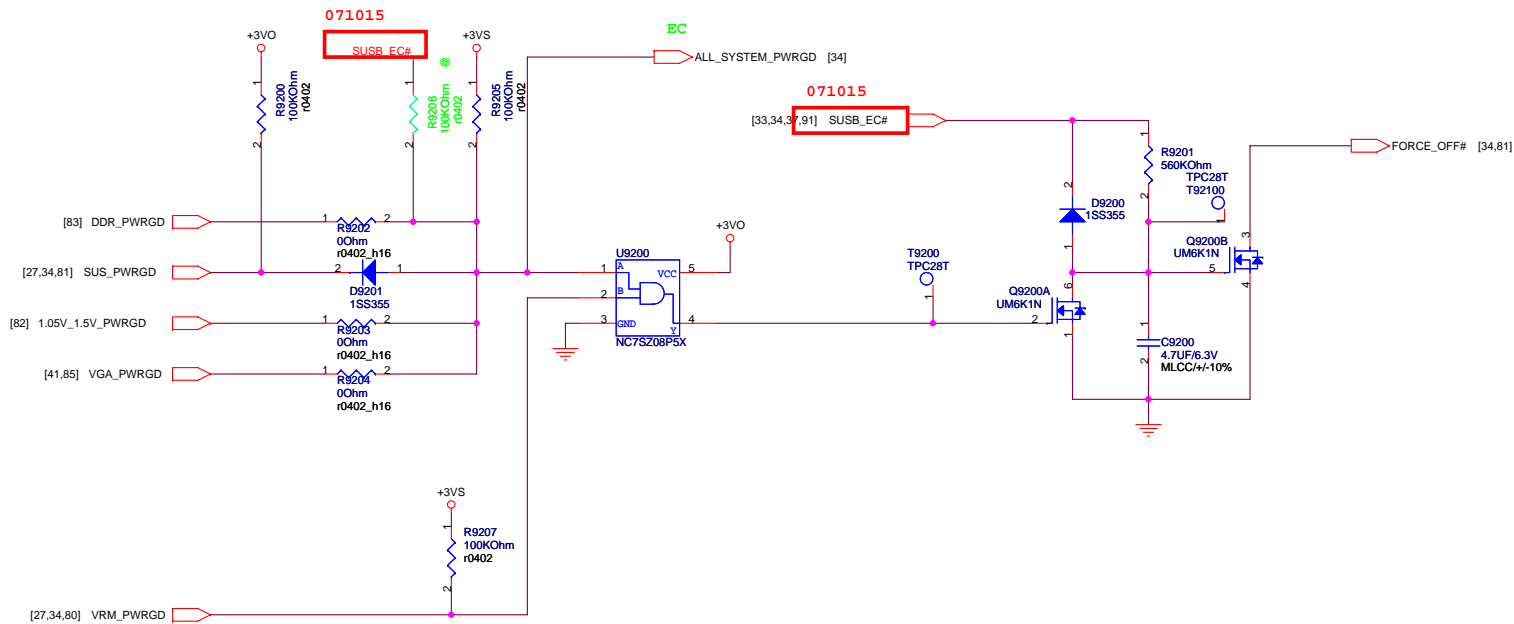
SUSB#_PWR POWER



SUSC#_PWR POWER

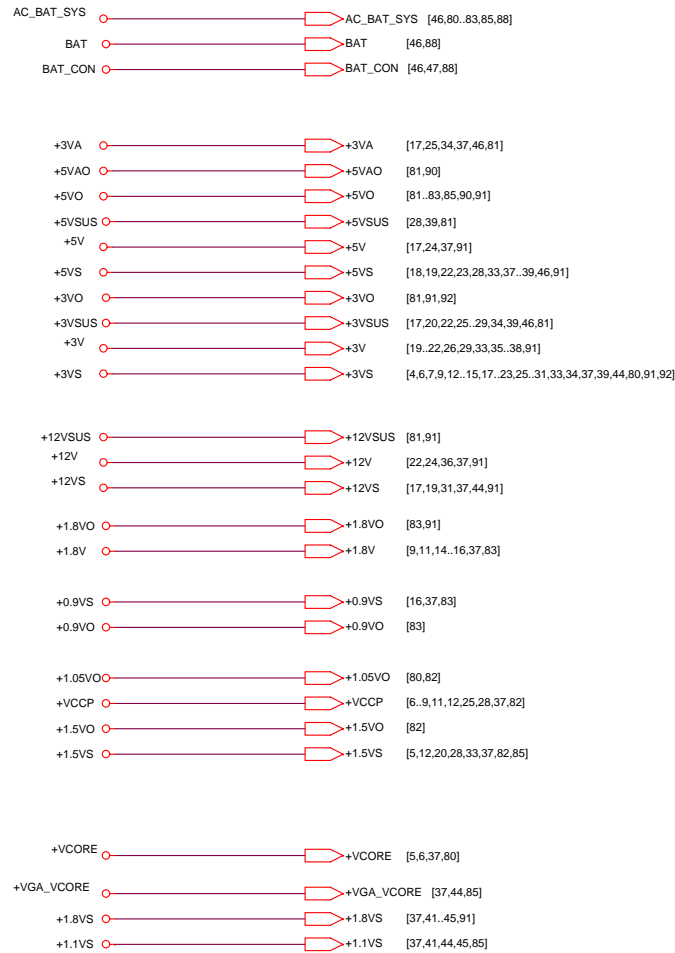


POWER GOOD DETECTOR



<Variant Name>

ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name	Rev	
Custom	F6V	1.0	
Date: Friday, September 26, 2008	Sheet	92	of 64



FOR POWER TEST

